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PROJ	<b>youyeetoo X1</b>
Title	JSL SOC-LPDDR4x CH0
Size A3	Document Number 4
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U1000C  
IC  
INS26356598

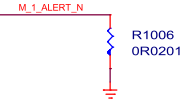
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BM51 LP4X\_3\_D028DDR\_1\_D060  
BJ51 LP4X\_3\_D027DDR\_1\_D059  
BL47 LP4X\_3\_D026DDR\_1\_D058  
BL49 LP4X\_3\_D025DDR\_1\_D057  
BM46 LP4X\_3\_D024DDR\_1\_D056  
BP59 LP4X\_3\_D023DDR\_1\_D055  
BP41 LP4X\_3\_D022DDR\_1\_D054  
BP44 LP4X\_3\_D021DDR\_1\_D053  
BM45 LP4X\_3\_D020DDR\_1\_D052  
BP45 LP4X\_3\_D019DDR\_1\_D051  
BM39 LP4X\_3\_D018DDR\_1\_D050  
BM44 LP4X\_3\_D017DDR\_1\_D049  
BM41 LP4X\_3\_D016DDR\_1\_D048  
BC47 LP4X\_3\_D015DDR\_1\_D047  
BC46 LP4X\_3\_D014DDR\_1\_D046  
BD49 LP4X\_3\_D013DDR\_1\_D045  
BF51 LP4X\_3\_D012DDR\_1\_D044  
BC51 LP4X\_3\_D011DDR\_1\_D043  
BF47 LP4X\_3\_D010DDR\_1\_D042  
BF49 LP4X\_3\_D009DDR\_1\_D041  
BF46 LP4X\_3\_D008DDR\_1\_D040  
BH39 LP4X\_3\_D007DDR\_1\_D039  
BH41 LP4X\_3\_D006DDR\_1\_D038  
BH44 LP4X\_3\_D005DDR\_1\_D037  
BF45 LP4X\_3\_D004DDR\_1\_D036  
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BF44 LP4X\_3\_D002DDR\_1\_D034  
BF41 LP4X\_3\_D001DDR\_1\_D033  
AG47 LP4X\_3\_D000DDR\_1\_D032  
AG46 LP4X\_2\_D031DDR\_1\_D031  
AG48 LP4X\_2\_D030DDR\_1\_D030  
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AB45 LP4X\_2\_D004DDR\_1\_D004  
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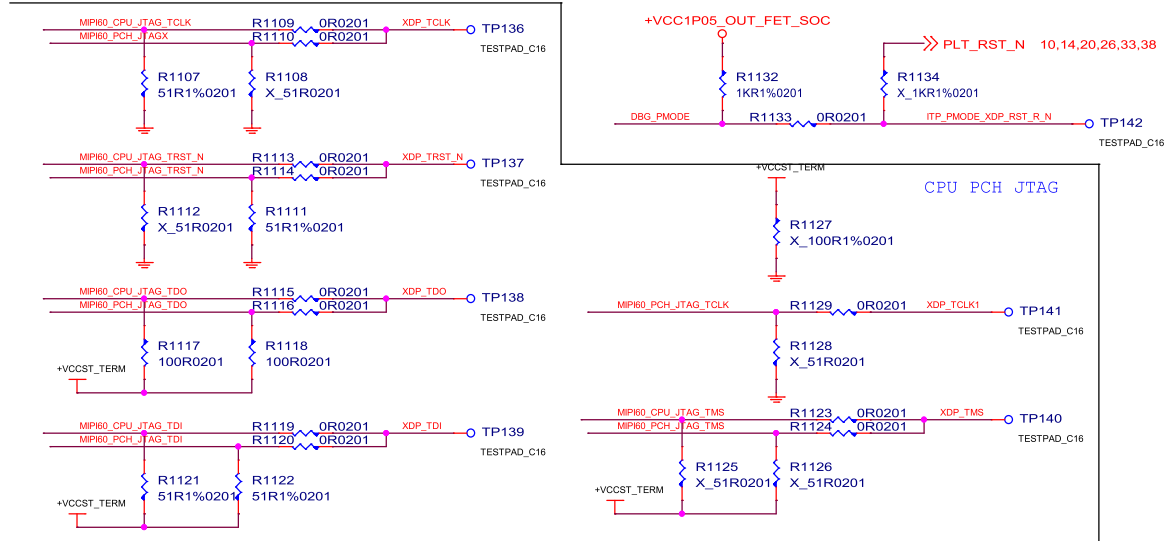
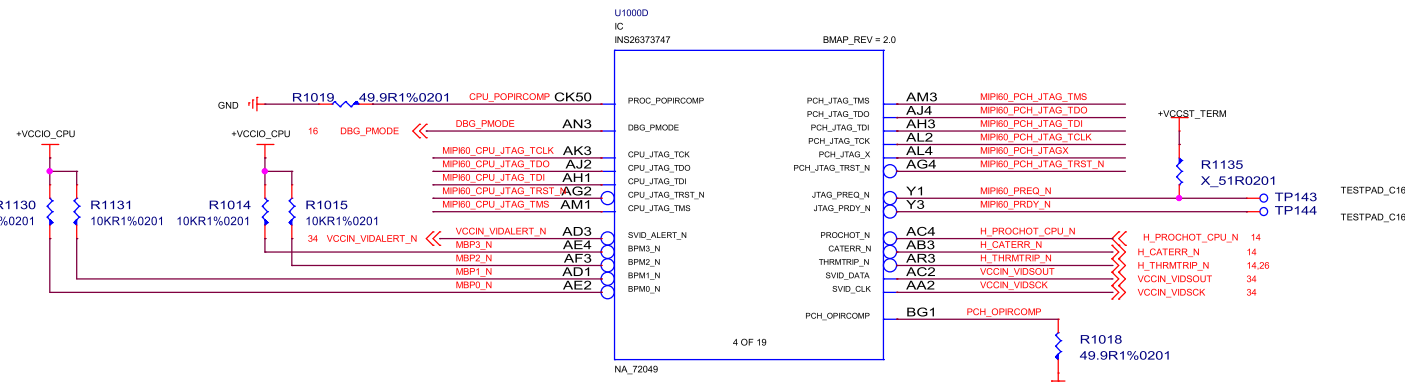
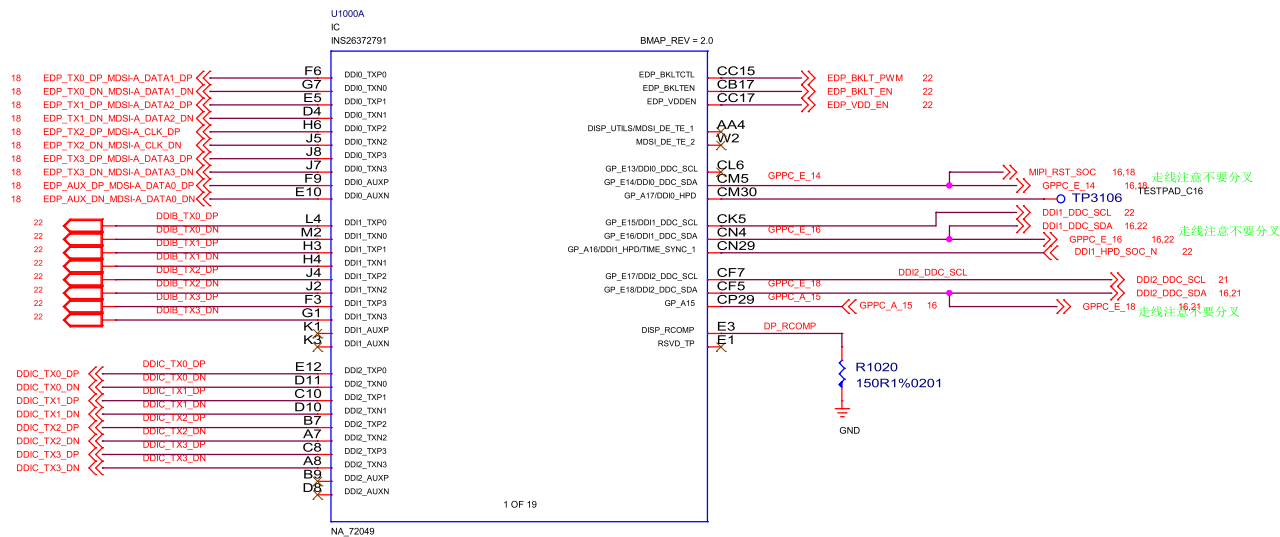
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NA\_72049

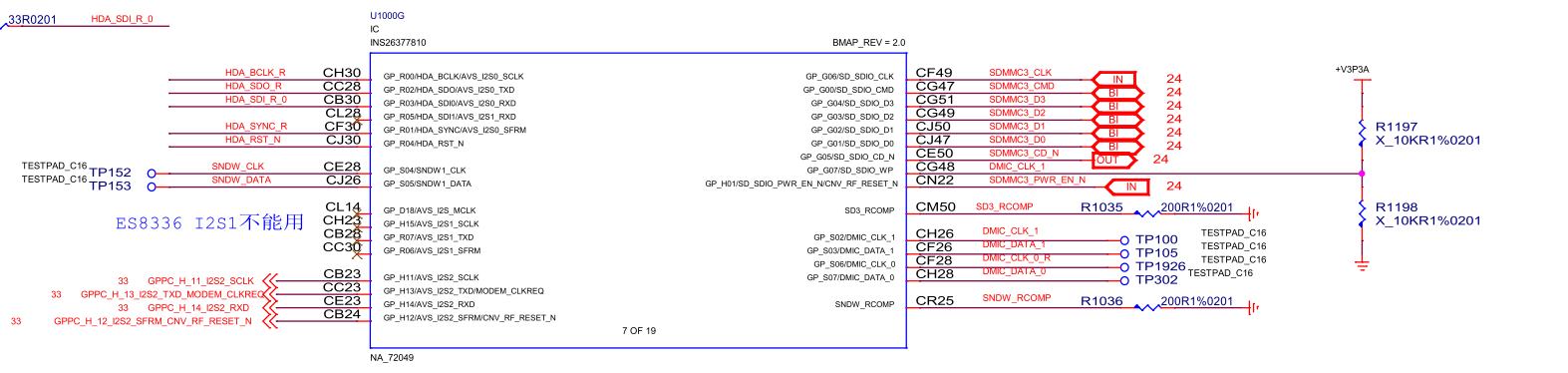
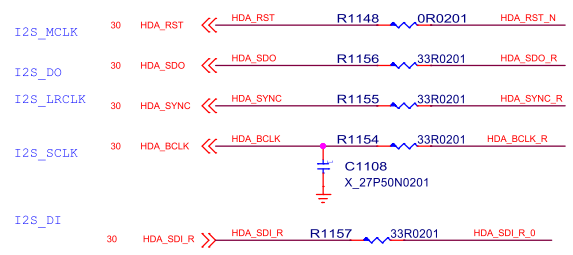
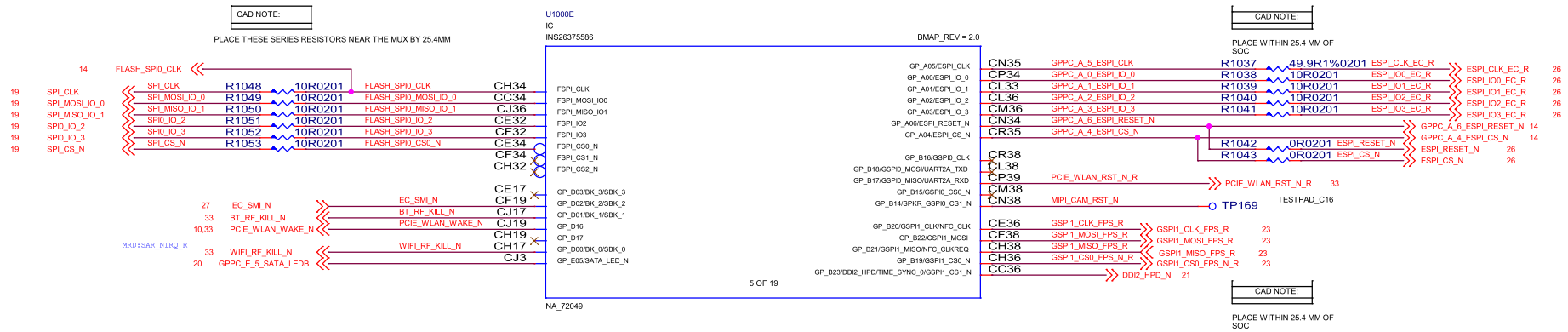
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LP4X\_2\_CLK\_DPDDR\_1\_CLK0\_DP AV48  
LP4X\_2\_CKE1 AY41  
LP4X\_2\_CKE0DDR\_1\_CKE0 AY42  
LP4X\_3\_CKE1DDR\_1\_CKE1 AY45  
LP4X\_3\_CKE0 BB44  
LP4X\_2\_CS1 AY50  
LP4X\_2\_CS0DDR\_1\_CS0\_N AW48  
LP4X\_3\_CS1DDR\_1\_CS1\_N BA51  
LP4X\_3\_CS0 AY47  
LP4X\_3\_CA0DDR\_1\_MA13 AT51  
LP4X\_3\_CA0DDR\_1\_BA0 AN51  
DDR\_1\_BG1 AP44  
LP4X\_2\_CASDDR\_1\_BG0 AT45  
LP4X\_3\_CA3DDR\_1\_MA16\_RAS\_N AR49  
LP4X\_3\_CA1DDR\_1\_MA16\_CAS\_N BA49  
LP4X\_3\_CA2DDR\_1\_MA14\_WE\_N AP50  
DDR\_1\_BA1 AN47  
DDR\_1\_MA12 AP45  
DDR\_1\_MA11 AP42  
DDR\_1\_MA10 AT48  
LP4X\_2\_CA1DDR\_1\_MA09 AT42  
LP4X\_2\_CA0DDR\_1\_MA08 AT41  
LP4X\_2\_CA4DDR\_1\_MA07 AT39  
LP4X\_2\_CA2DDR\_1\_MA06 AT44  
LP4X\_2\_CA0DDR\_1\_MA05 AP41  
DDR\_1\_MA04 AY44  
DDR\_1\_MA03 BB42  
LP4X\_3\_CASDDR\_1\_MA02 AR47  
DDR\_1\_MA01 AN49  
DDR\_1\_MA00 AP48  
DDR\_1\_ODT1 AM48  
DDR\_1\_ODT0 BA48  
LP4X\_3\_D0S3\_DPDDR\_1\_D0S7\_DP BK48  
LP4X\_3\_D0S3\_DNDDR\_1\_D0S7\_DN BK50  
LP4X\_3\_D0S2\_DPDDR\_1\_D0S6\_DP BP42  
LP4X\_3\_D0S2\_DNDDR\_1\_D0S6\_DN BM42  
LP4X\_3\_D0S1\_DPDDR\_1\_D0S5\_DP BE48  
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LP4X\_3\_D0S0\_DPDDR\_1\_D0S4\_DP BF42  
LP4X\_3\_D0S0\_DNDDR\_1\_D0S4\_DN BF42  
LP4X\_2\_D0S3\_DPDDR\_1\_D0S3\_DP AJ48  
LP4X\_2\_D0S3\_DNDDR\_1\_D0S3\_DN AJ50  
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LP4X\_2\_D0S2\_DNDDR\_1\_D0S2\_DN AK42  
LP4X\_2\_D0S1\_DPDDR\_1\_D0S1\_DP AC48  
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LP4X\_2\_D0S0\_DPDDR\_1\_D0S0\_DP AD42  
LP4X\_2\_D0S0\_DNDDR\_1\_D0S0\_DN AB42  
DDR\_1\_PAR BB45  
DDR\_1\_ACT\_N AP39  
DDR\_1\_ALERT\_N AY39



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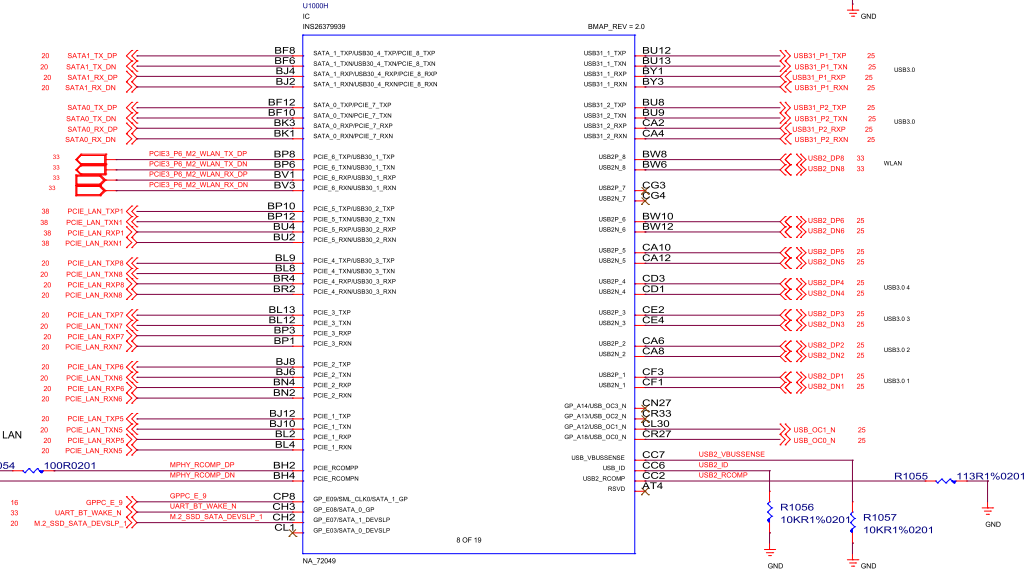
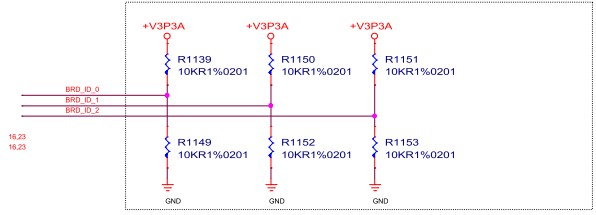
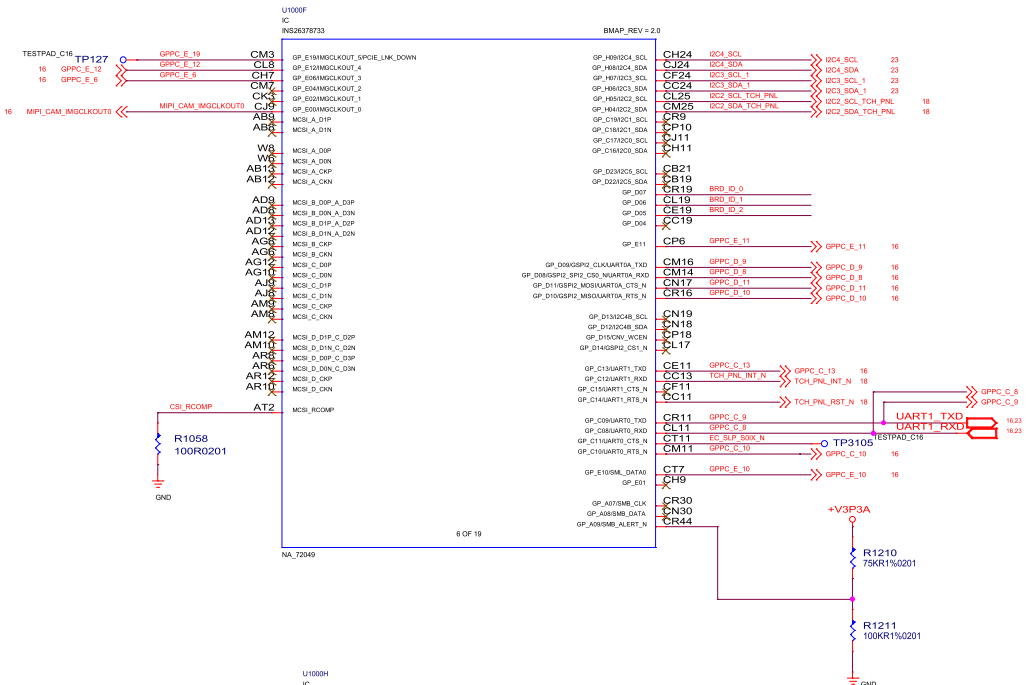
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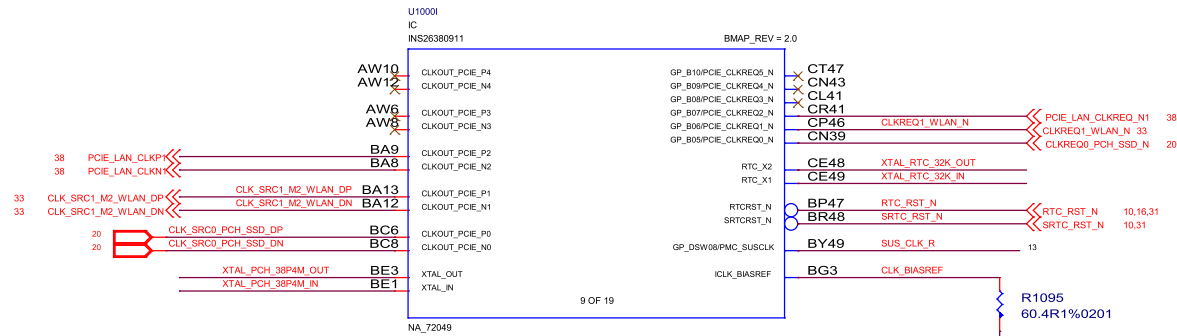
**PROJ youyeetoo X1**

Title JSL SOC-SPI-AUDIO

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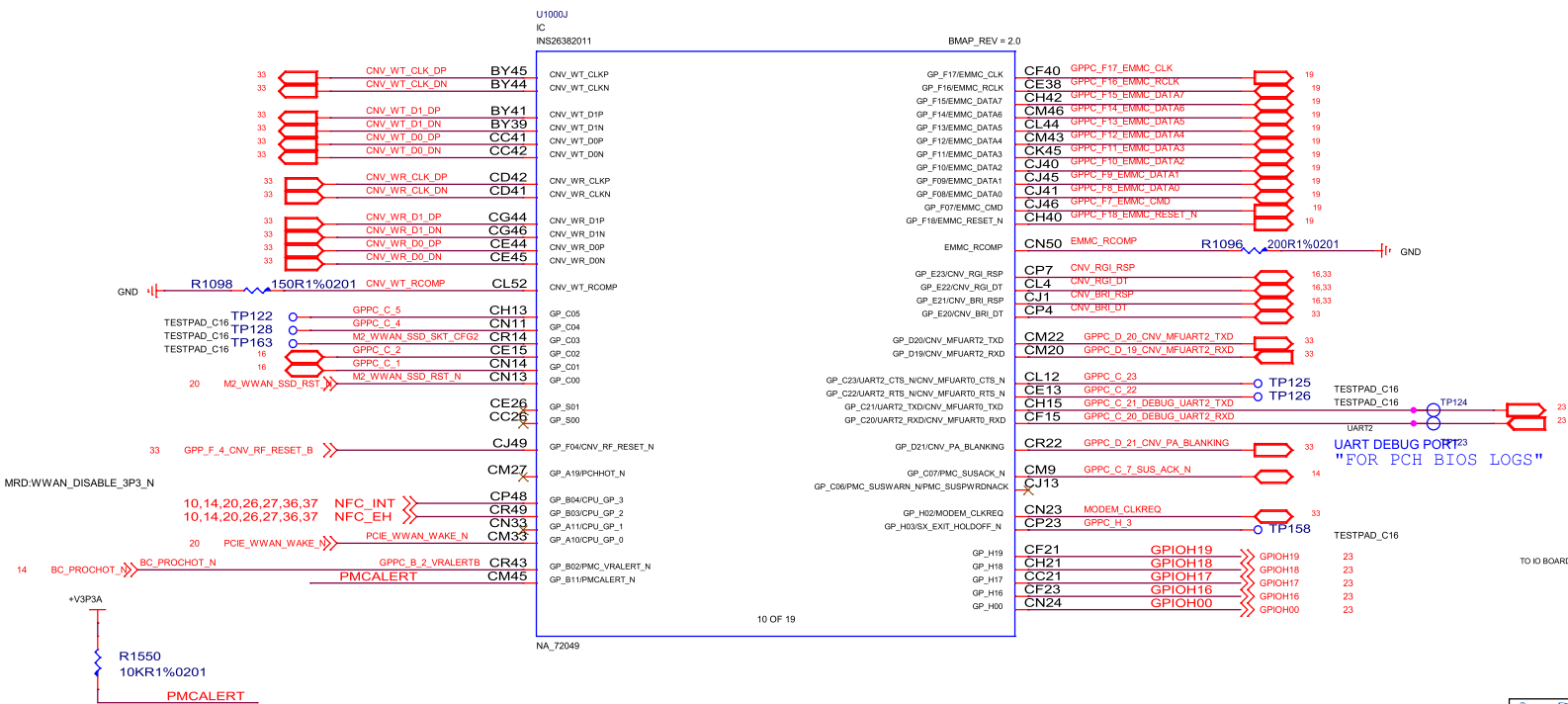
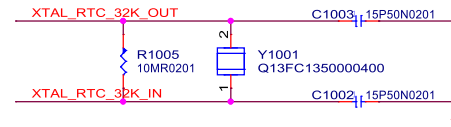
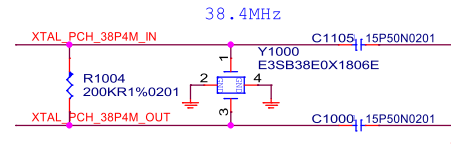
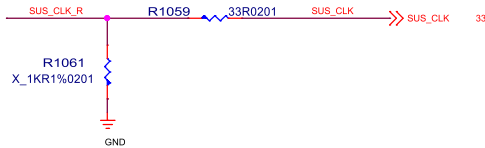
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CAD NOTE:

PLACE R5711 & R189 WITHIN 50.8MM OF SOC



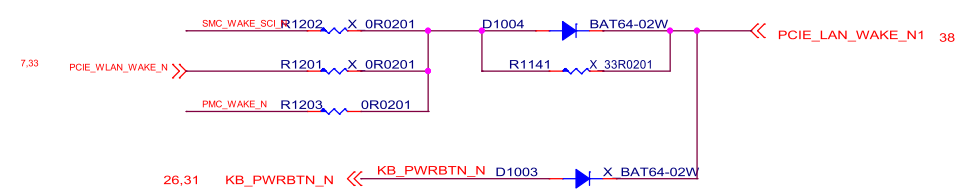
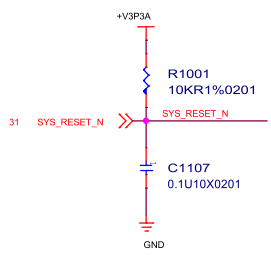
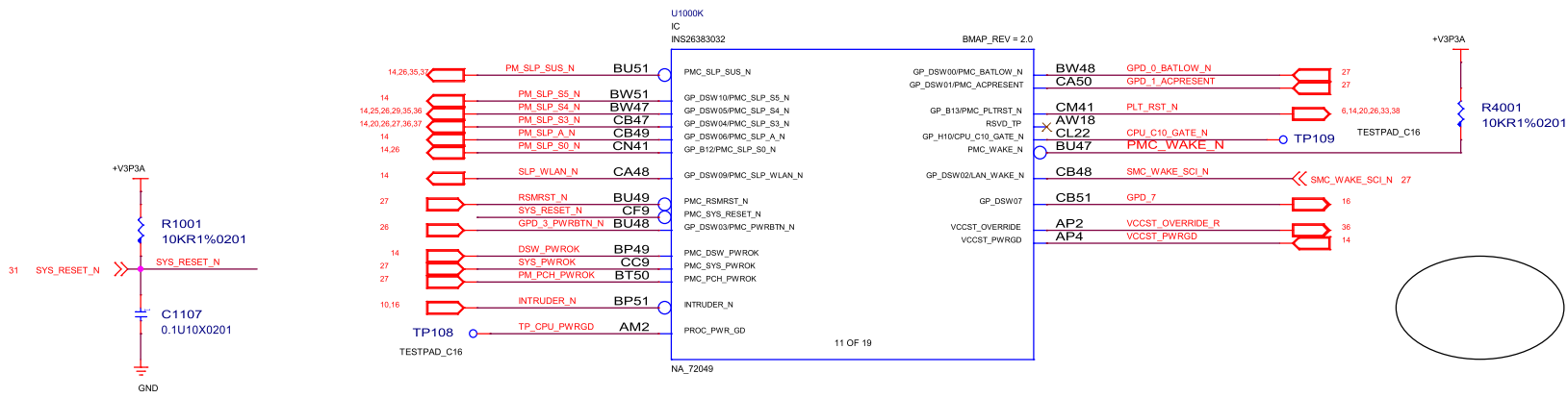
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TO IO BOARD

UART2  
"FOR PCH BIOS LOGS"

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**SPI VCCSSIO VOLTAGE CONFIGURATION**

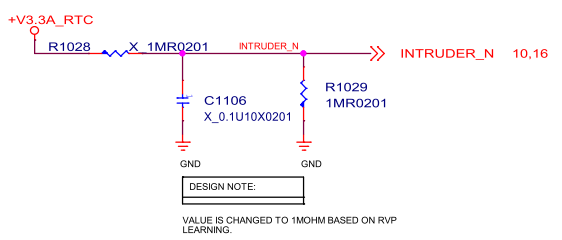
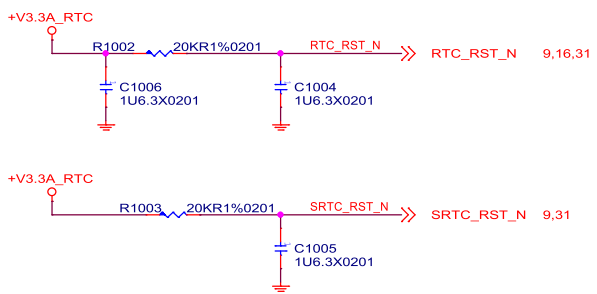
0 = SPI OPERATION VOLTAGE IS 3.3V (10 KOHM PULL-DOWN TO GND)

1 = SPI OPERATION VOLTAGE IS 1.8V (1 MOHM PULL-UP TO VCCRTC)

NO INTERNAL PU/PD

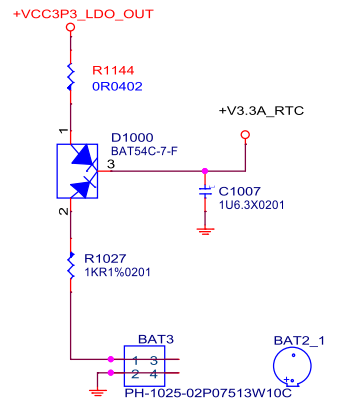
SAMPLING DSW\_PWROK

**RTC Circuit**

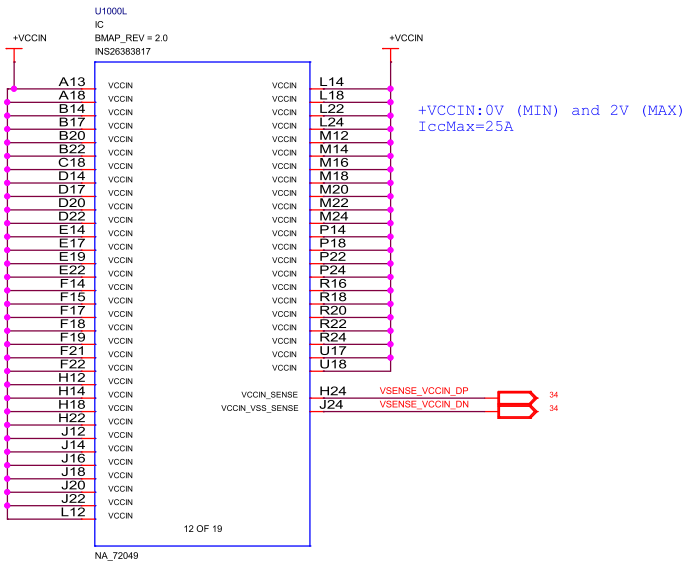


DESIGN NOTE:

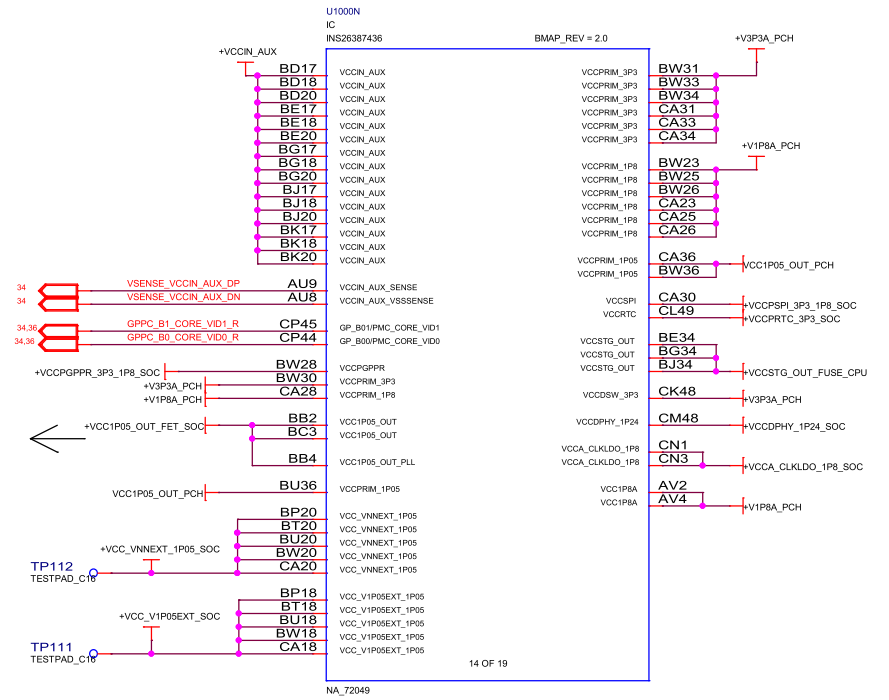
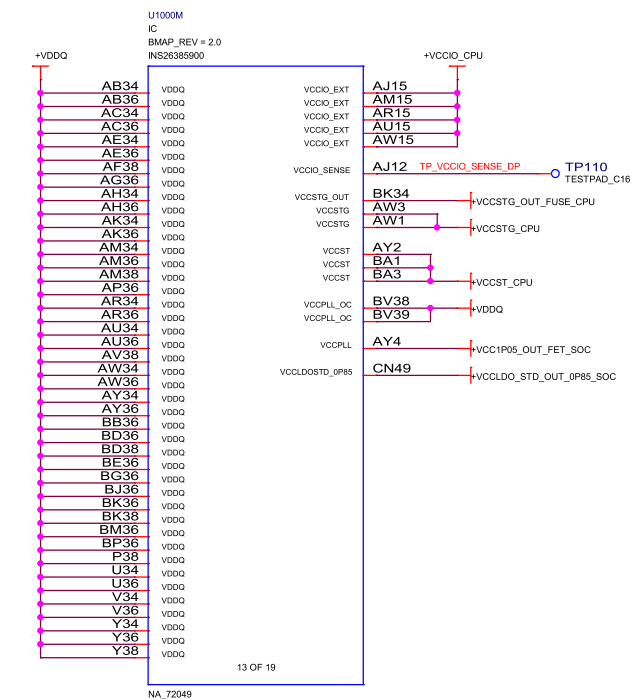
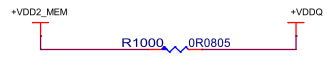
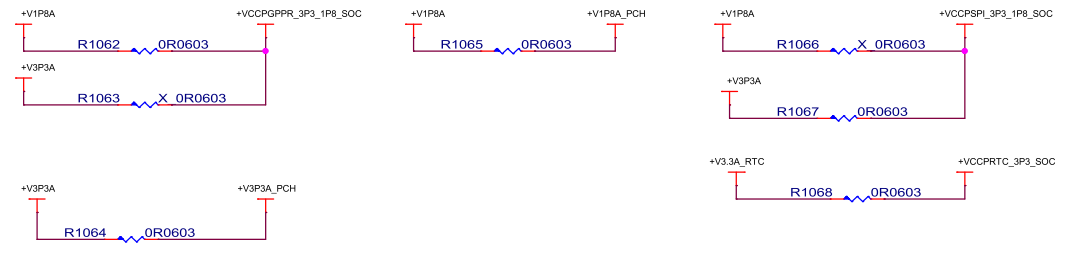
VALUE IS CHANGED TO 1MOHM BASED ON RVP LEARNING.



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+VCCIN:0V (MIN) and 2V (MAX)  
IccMax=25A

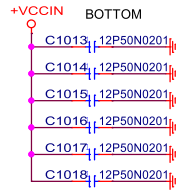


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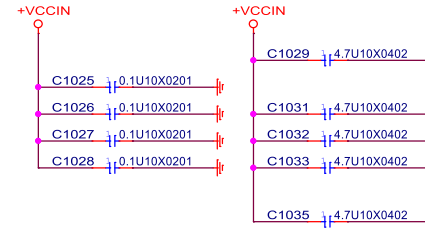
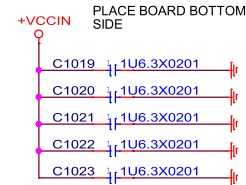
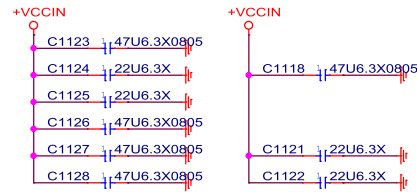




EMC CAPS - PLACE <5MM FROM SOC VCCIN

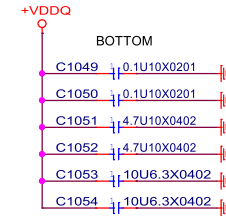
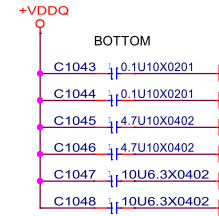
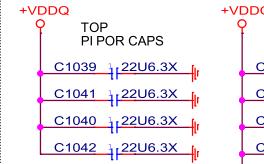
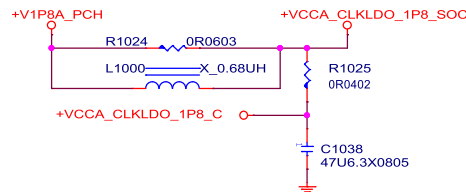
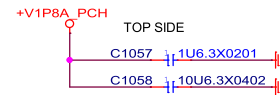
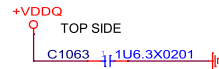
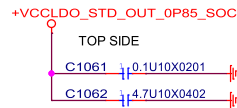
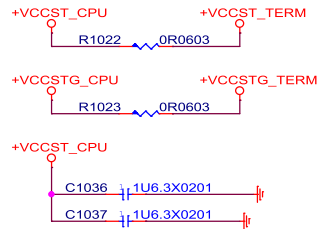


PLACE BOARD TOP SIDE

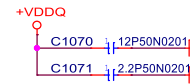
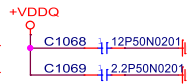
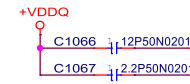
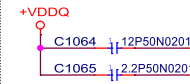


VCCSFR, VCCSTG, VCCST

TOP SIDE  
PI POR CAPS  
1 X 0402\_1UF  
+VCCST\_CPU

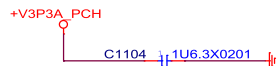
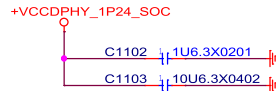
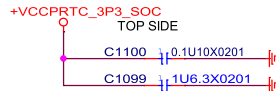
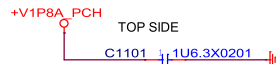
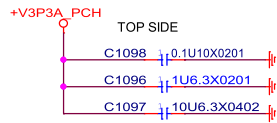


EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART



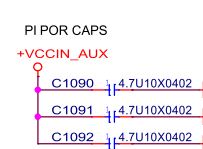
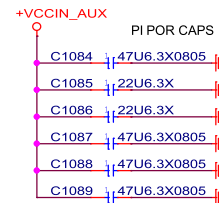
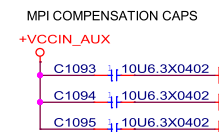
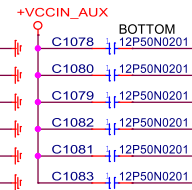
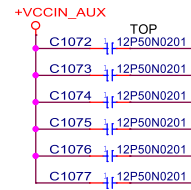
CPU CAP

PCH CAP



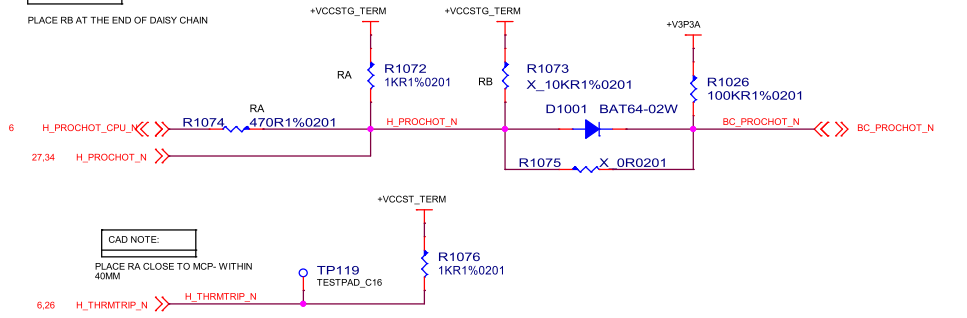
CAD NOTE:  
PLACE CAP C3F7 NEAR TO CK48 PIN OF SOC

EMC CAPS - PLACE <5MM FROM SOC VCCIN\_AUX



CAD NOTE:

PLACE RB AT THE END OF DAISY CHAIN

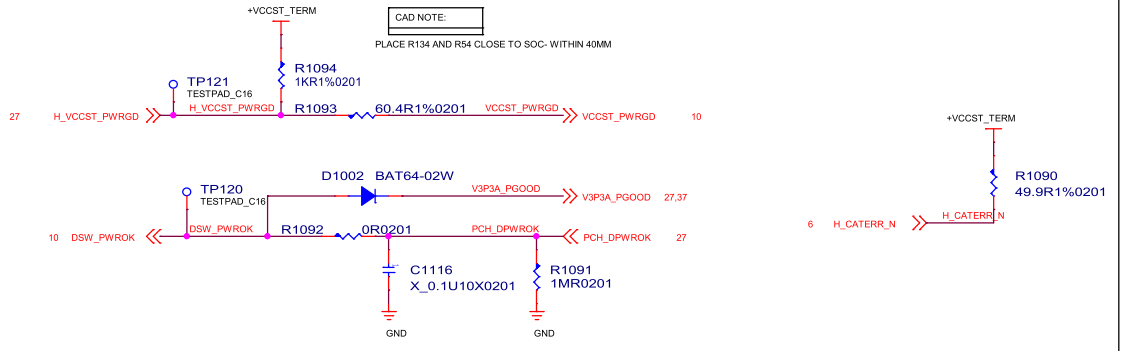


CAD NOTE:

PLACE RA CLOSE TO MCP- WITHIN 40MM

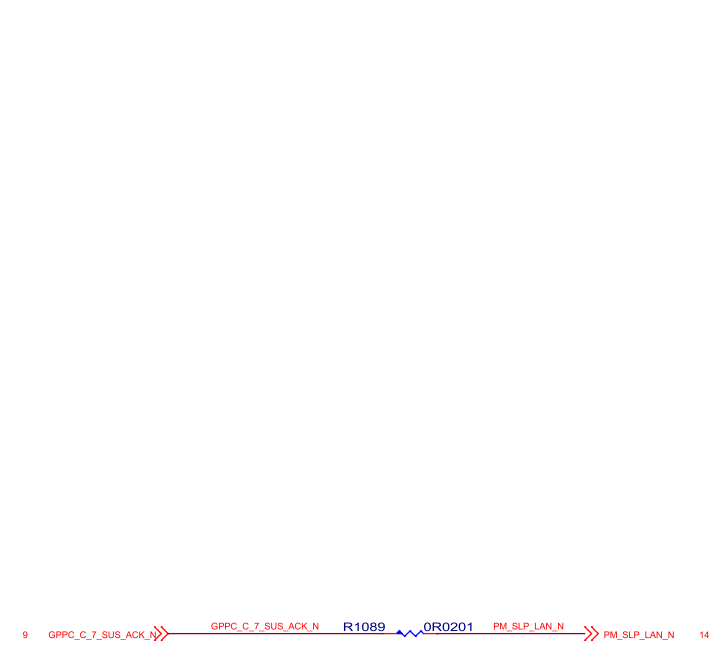
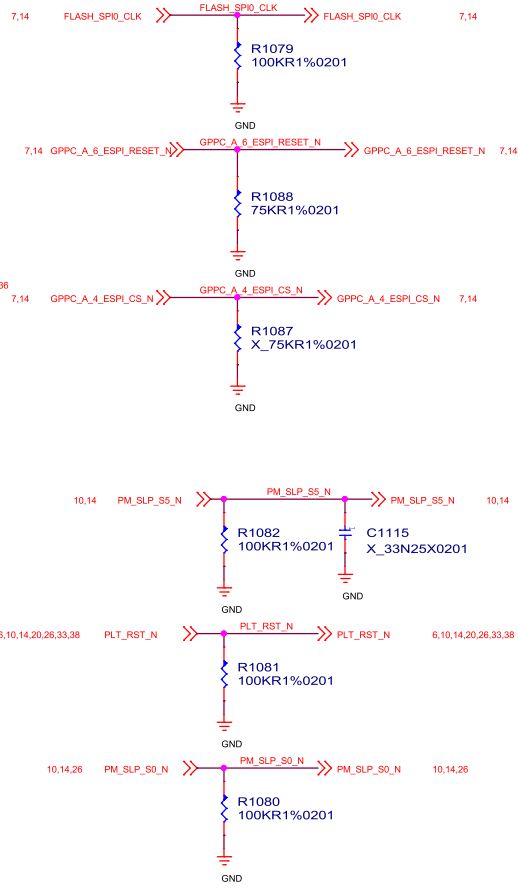
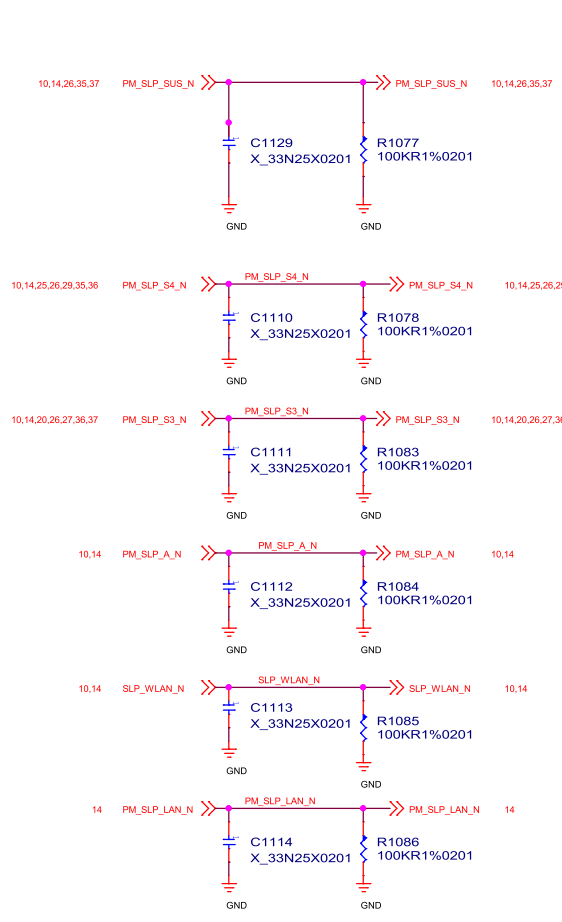
CAD NOTE:

PLACE R134 AND R54 CLOSE TO SOC- WITHIN 40MM

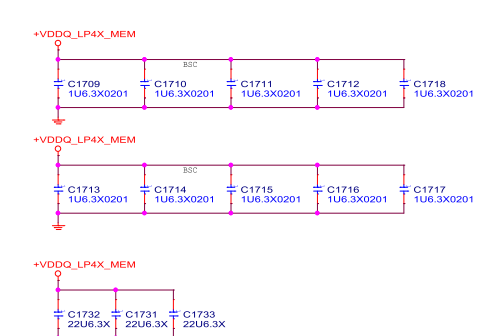
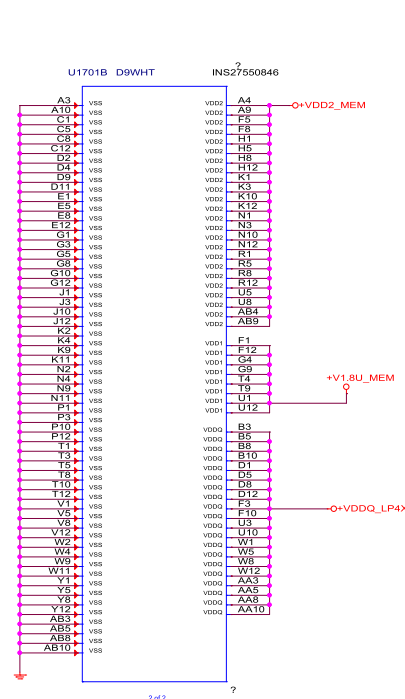
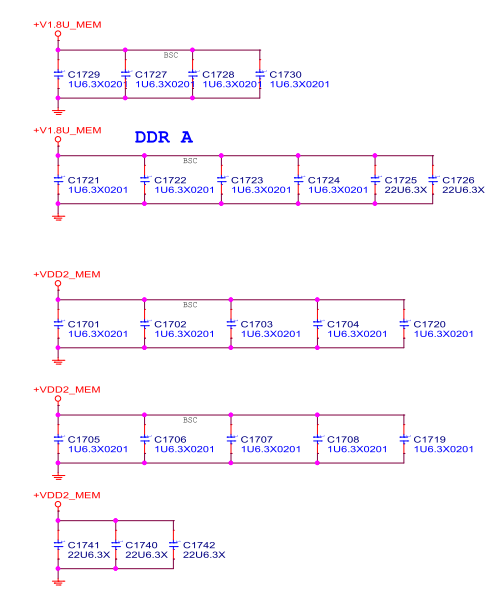
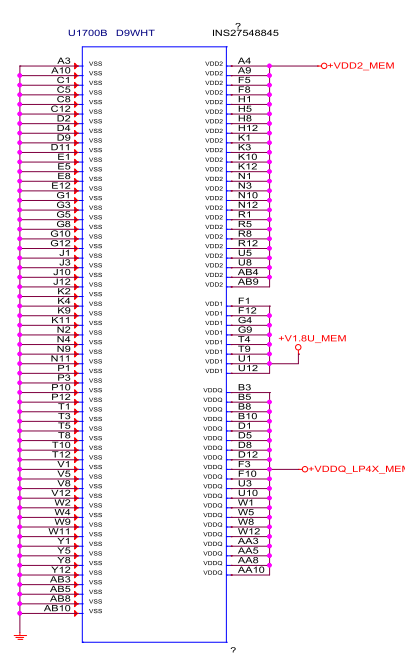
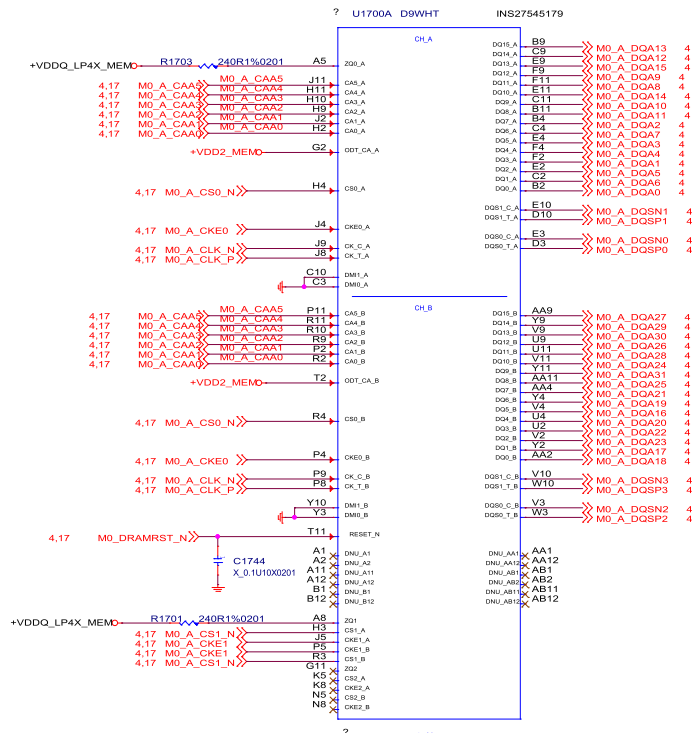


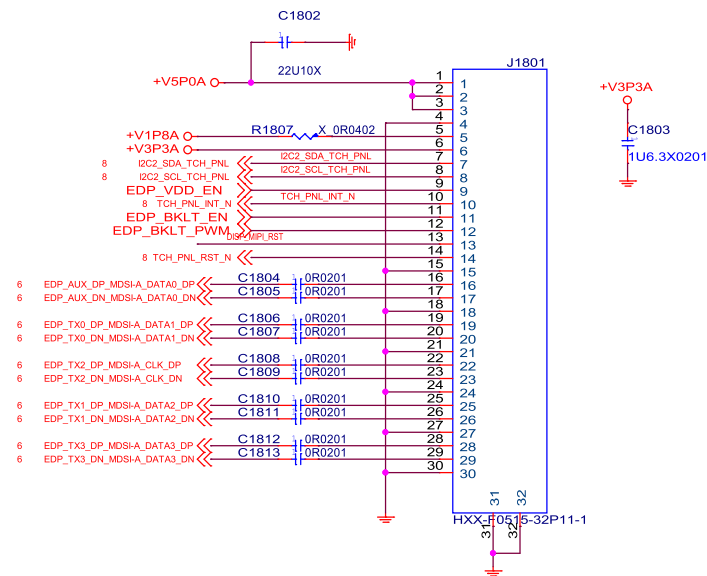
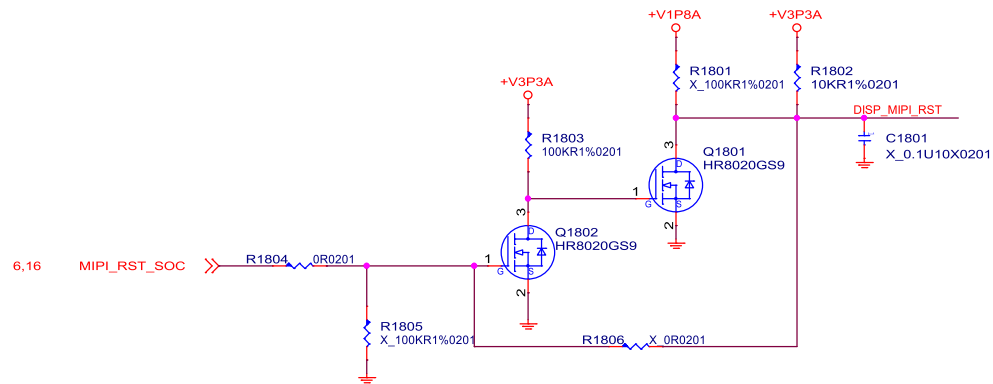
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PAGE\_TITLE=CPU SIDE BANDS



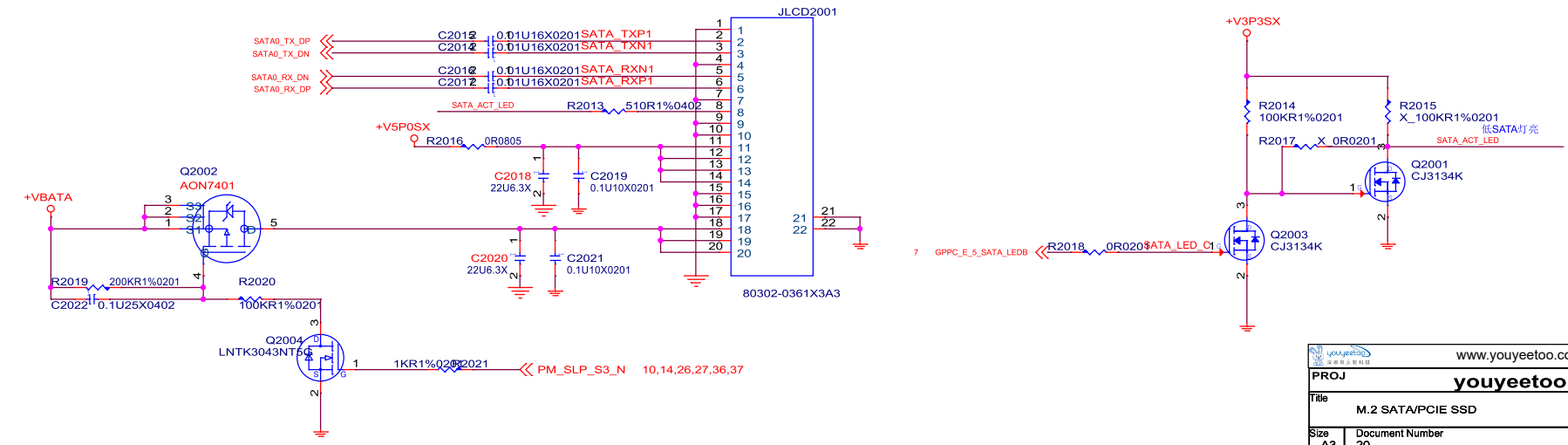
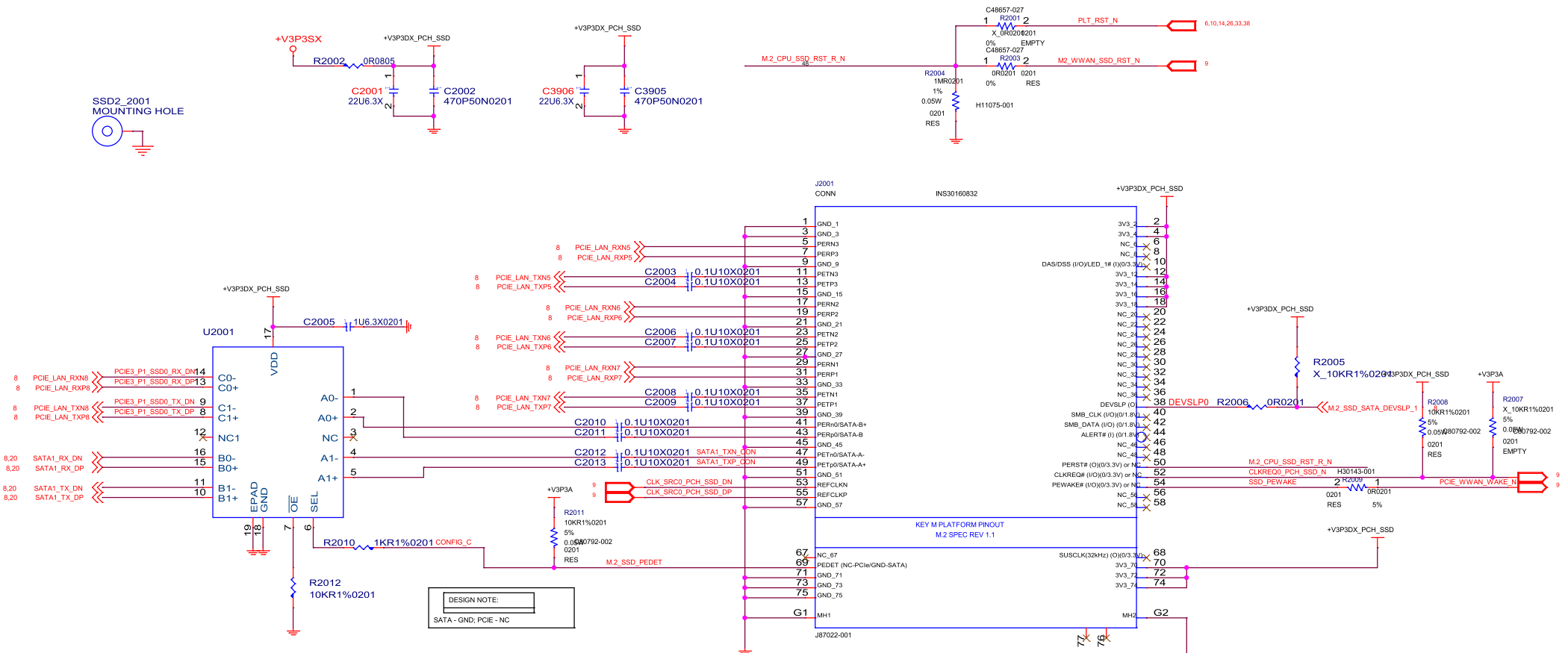
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PROJ	<b>youyeetoo X1</b>
Title	JSL SIDE BANDS-PCH GLITCH MI
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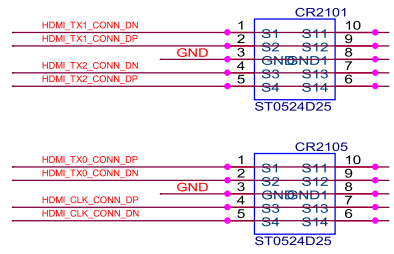
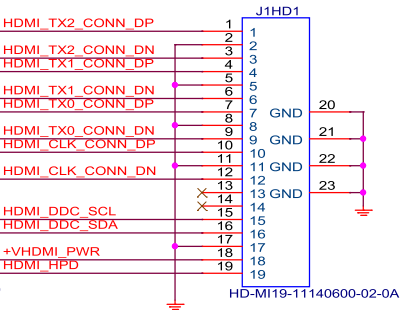
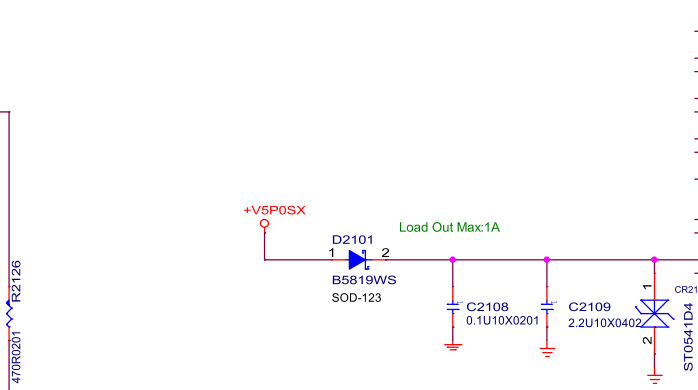
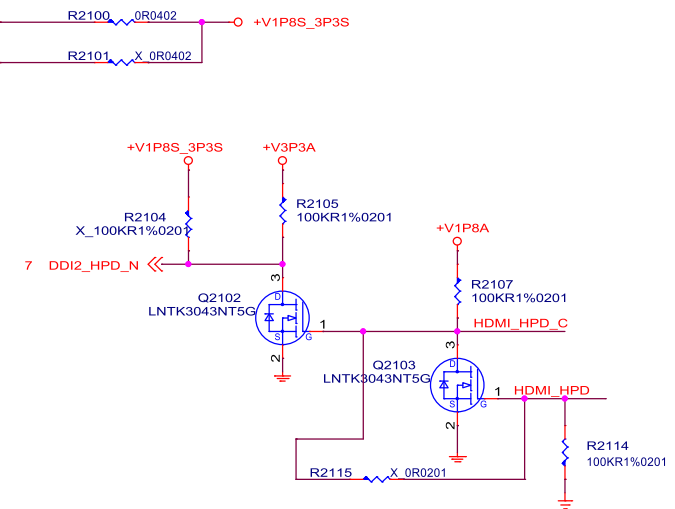
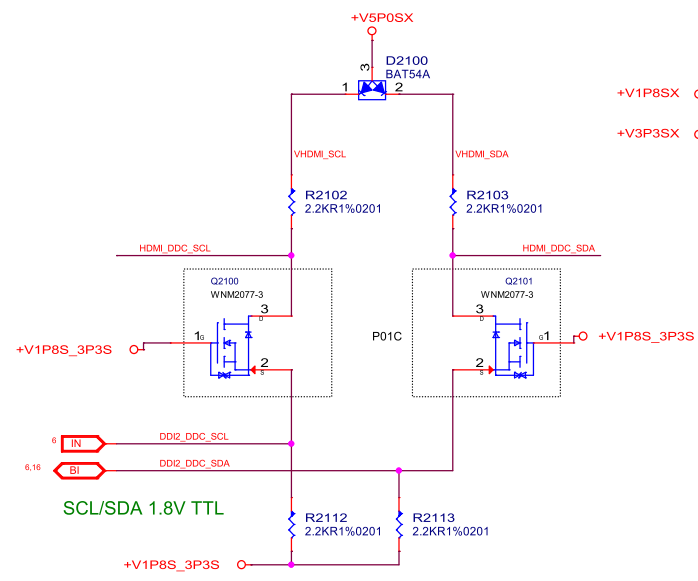
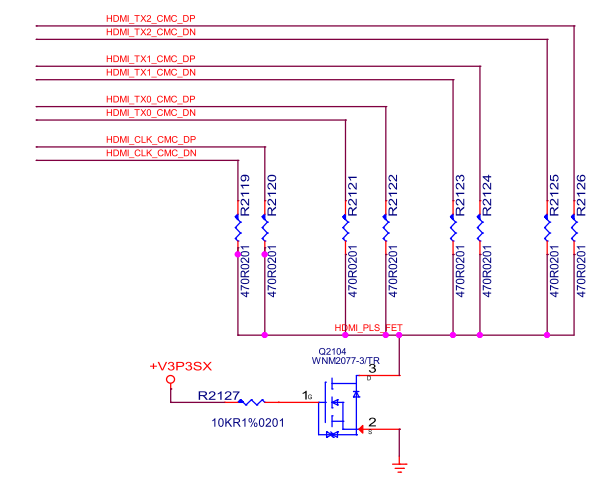
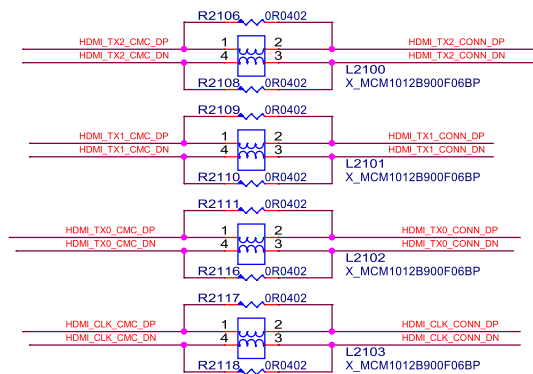
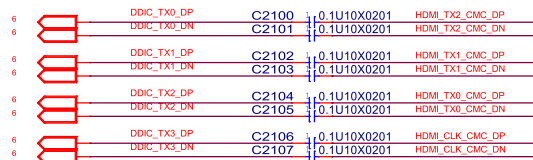


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PROJ	youyeetoo X1
Title	LPDDR4x_376ball CHB
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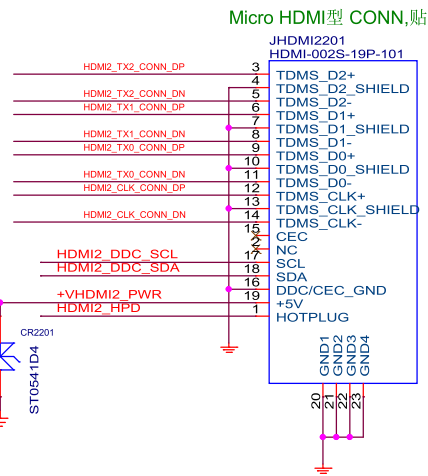
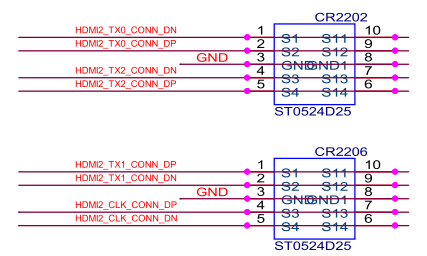
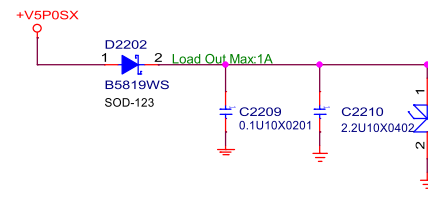
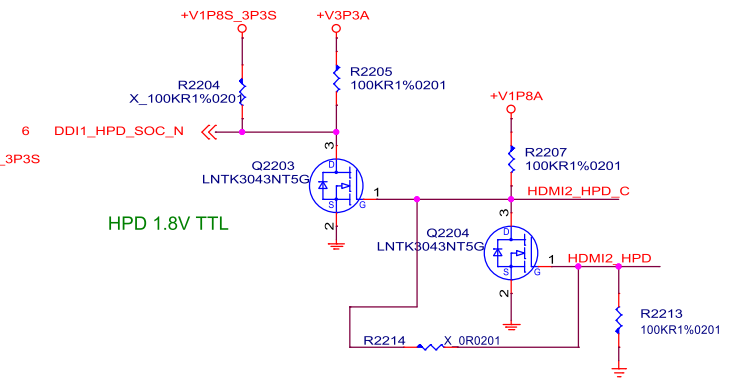
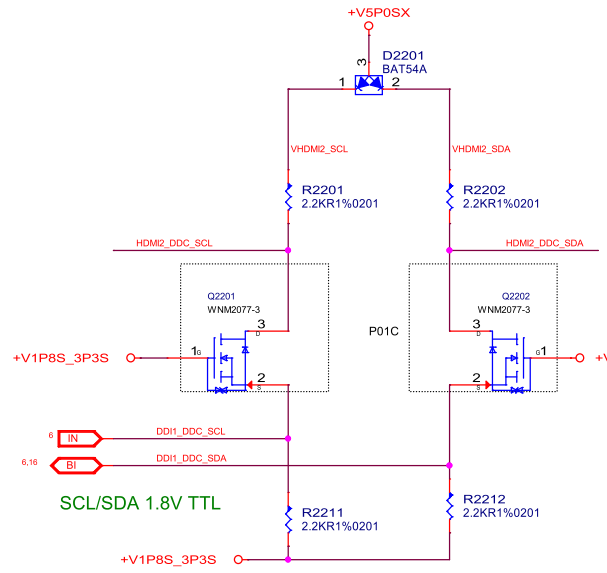
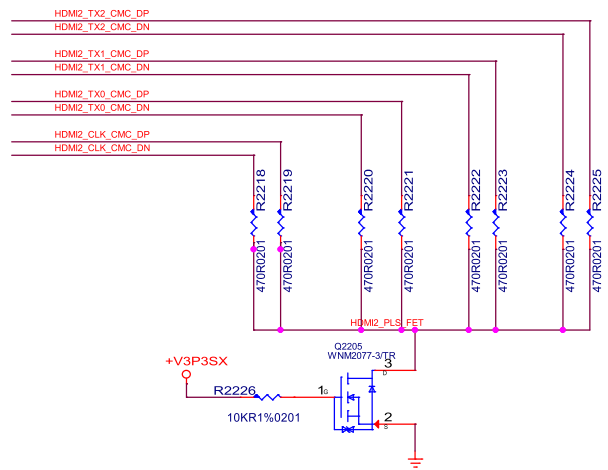
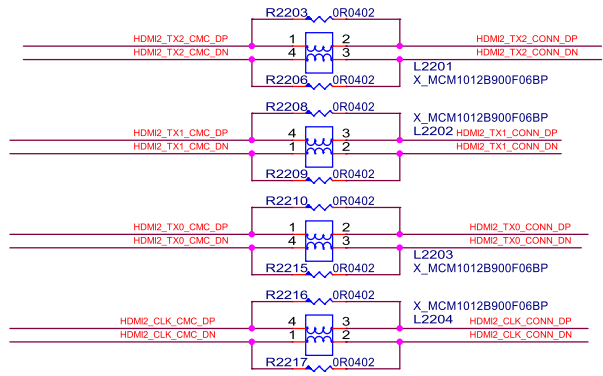
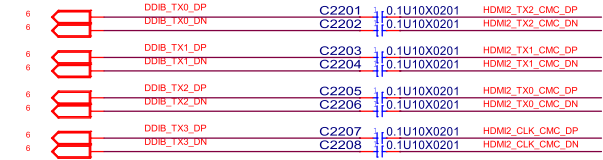


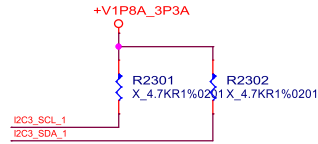
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Size A3	Document Number 20
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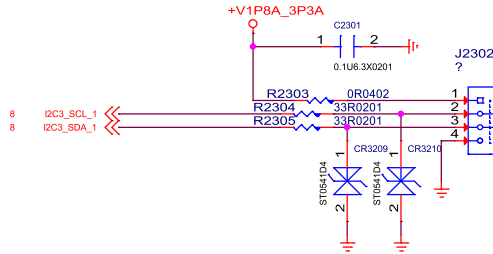
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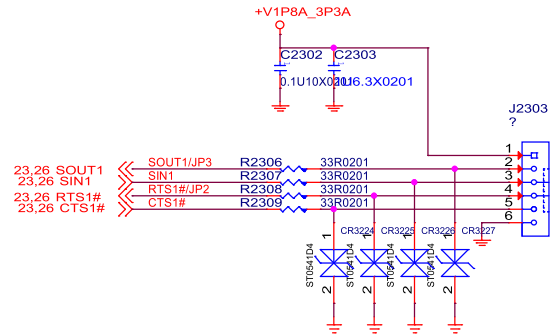


I2C接口



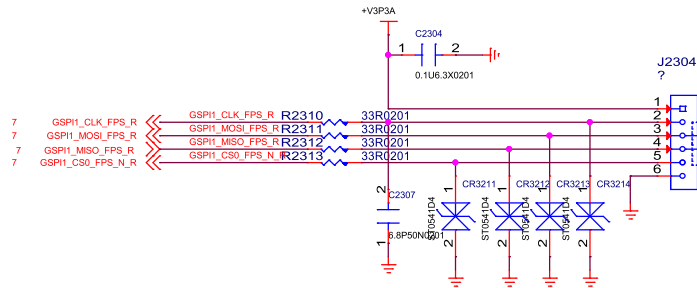
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UART1



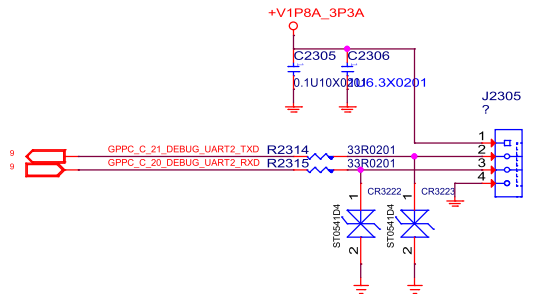
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SPI接口



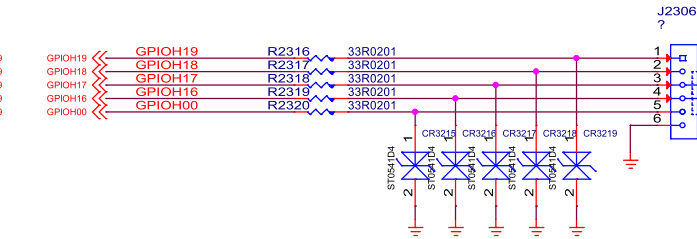
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UART2



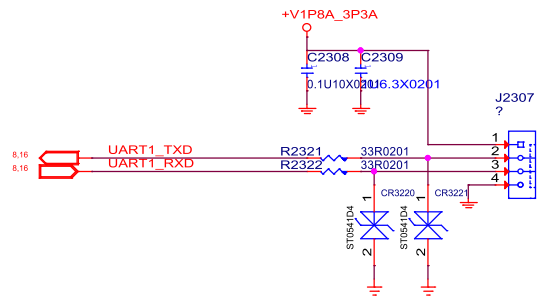
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GPIO接口

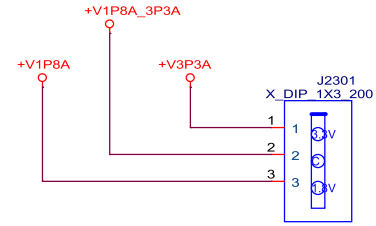
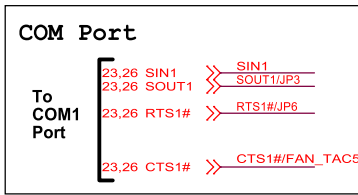


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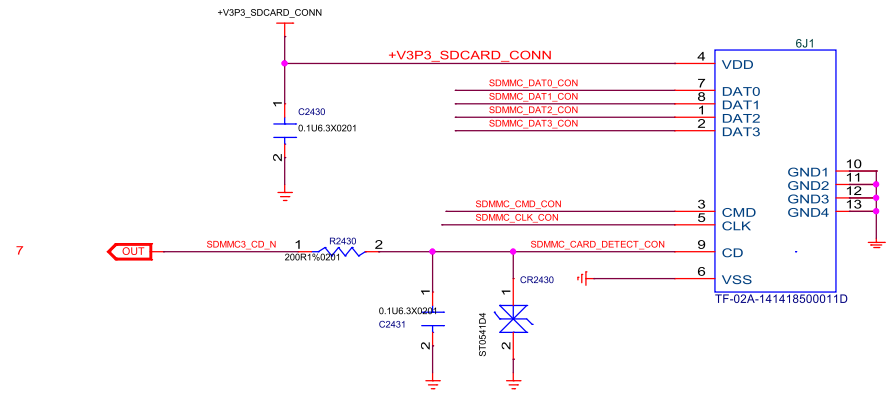
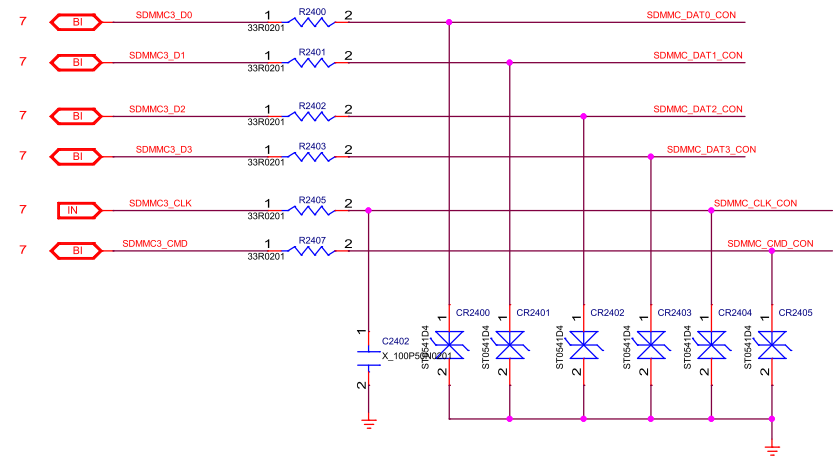
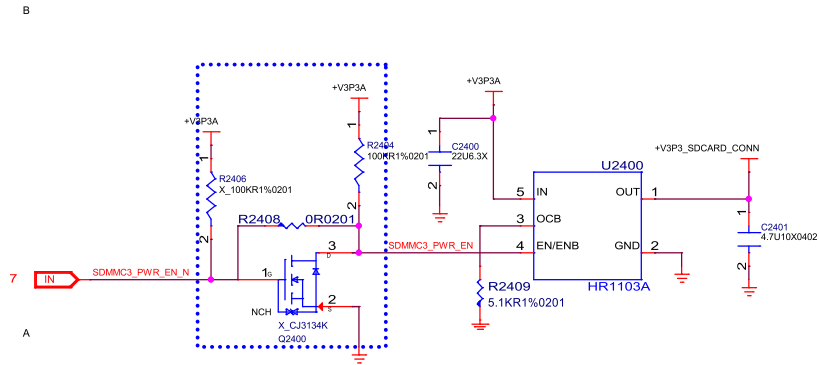
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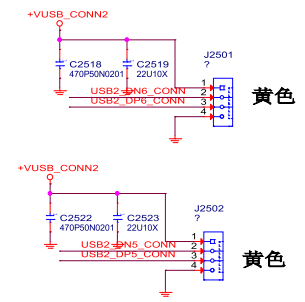
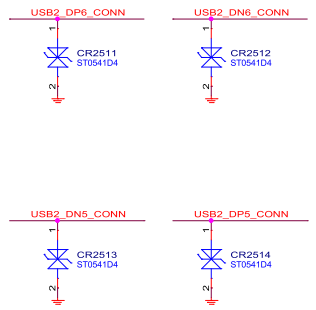
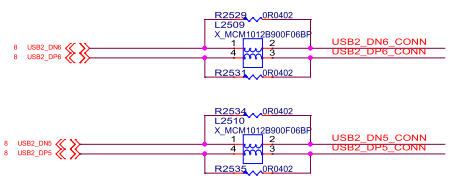
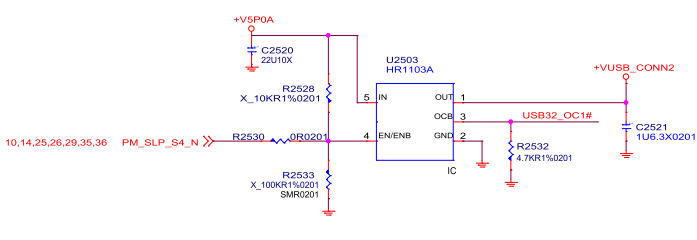
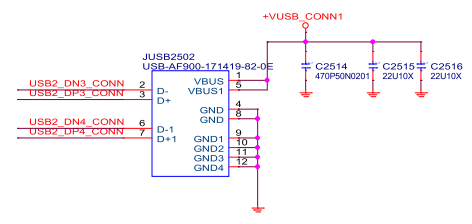
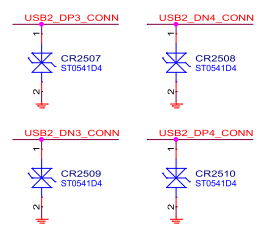
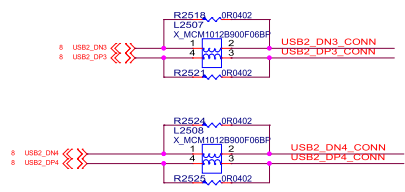
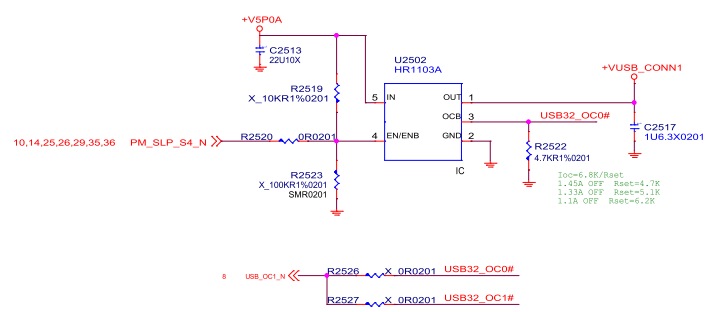
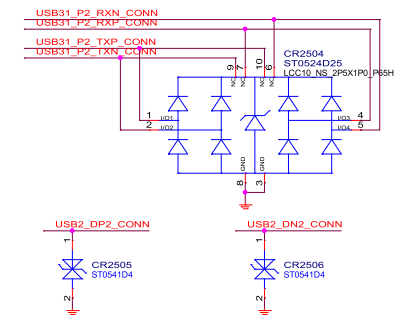
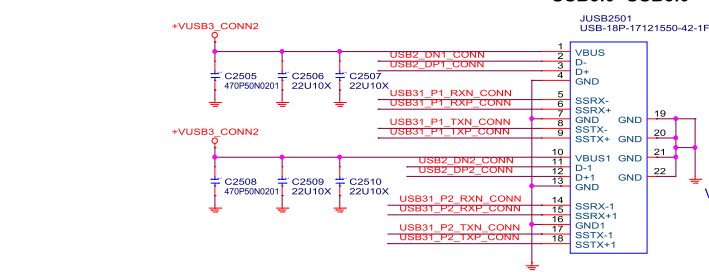
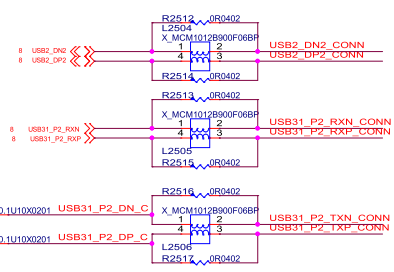
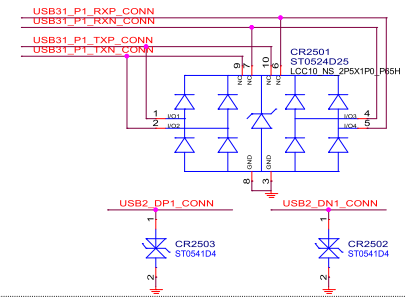
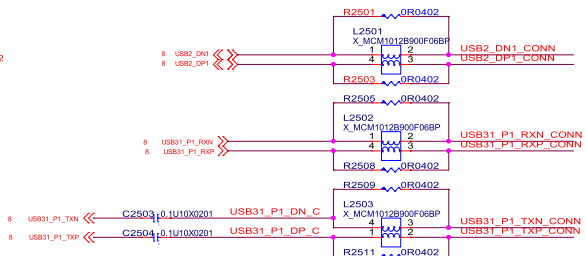
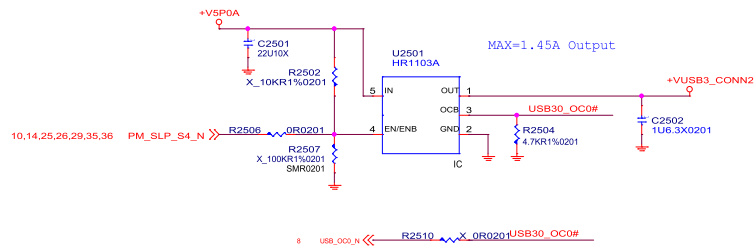


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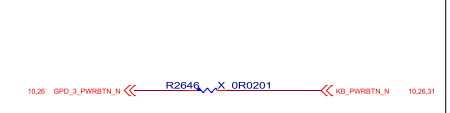
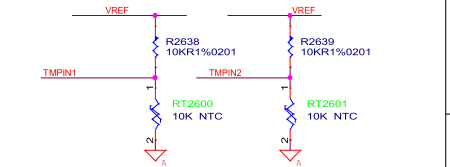
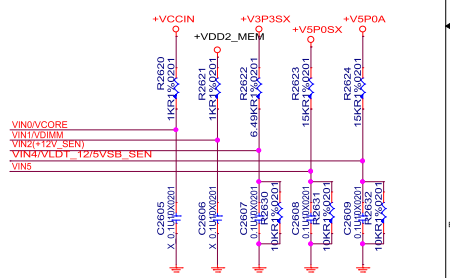
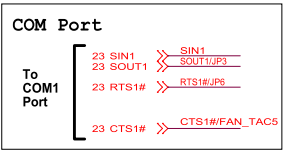
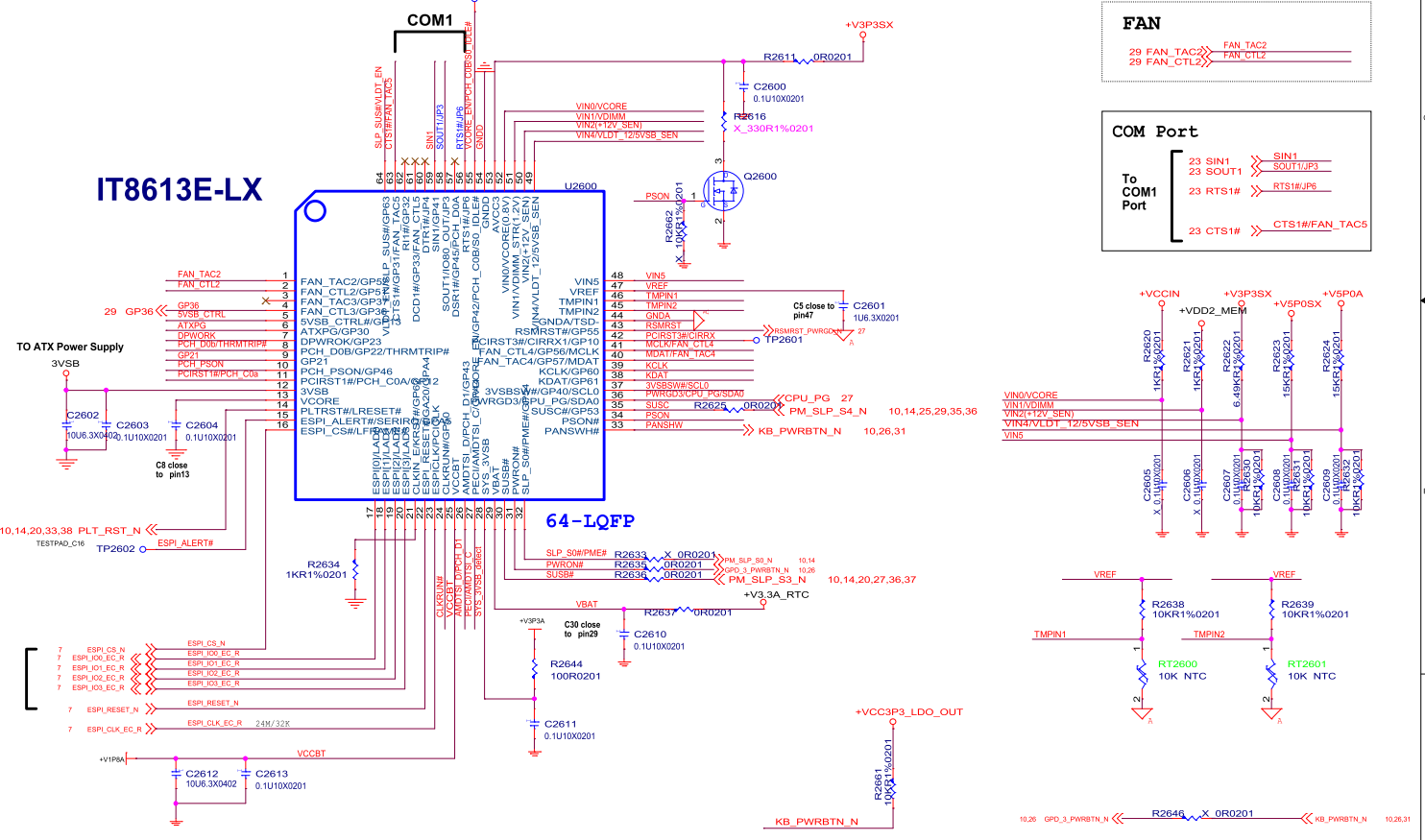
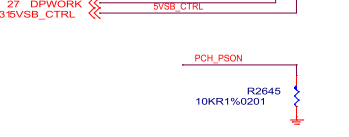
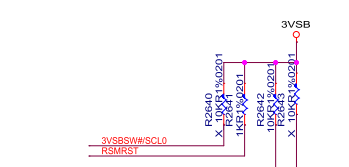
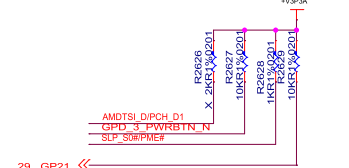
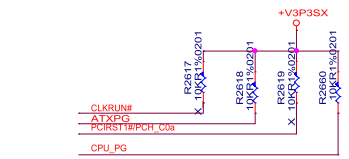
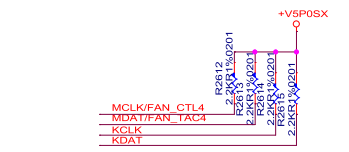
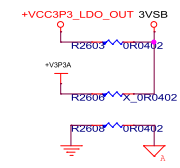


# USB2.0 TO SD Part




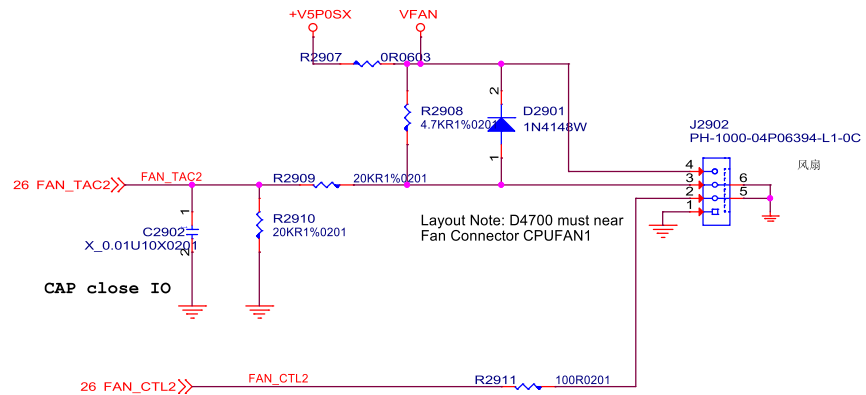
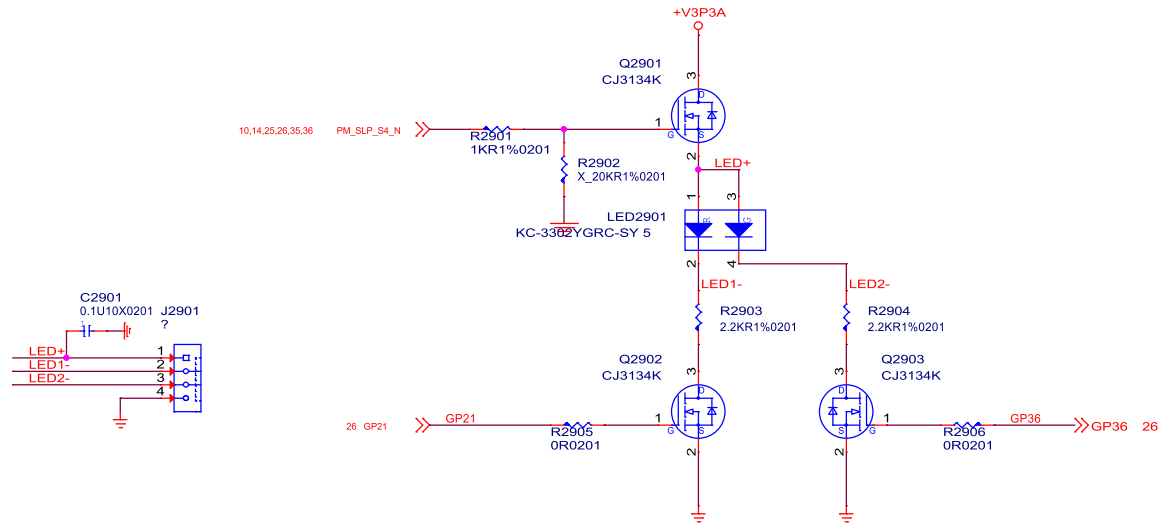


In DSW mode, SLP\_SUS can't floating  
 10,14,35,37 PM\_SLP\_SUS\_N >> R2609\_0R0201 SLP\_SUS#VLDT\_EN  
 6,14 H\_THRMTRIP\_N >> don't pull high THRMTRIP#PCH\_D0B#THRMTRIP#  
 12 H\_PECCI >> 0R0201\_R2610 PECCIAMDTSL\_C

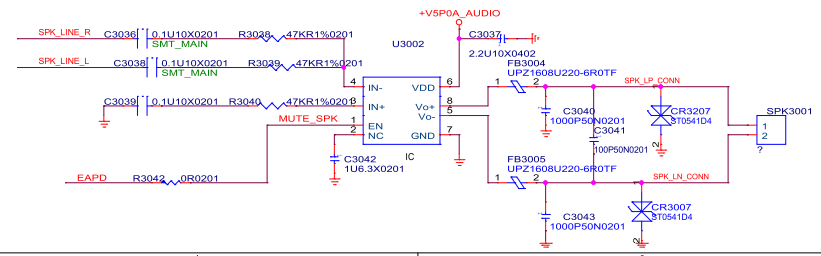
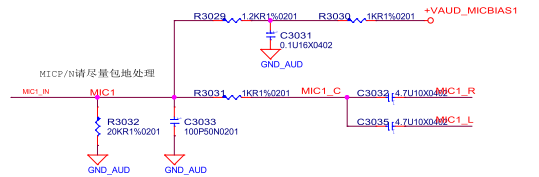
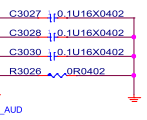
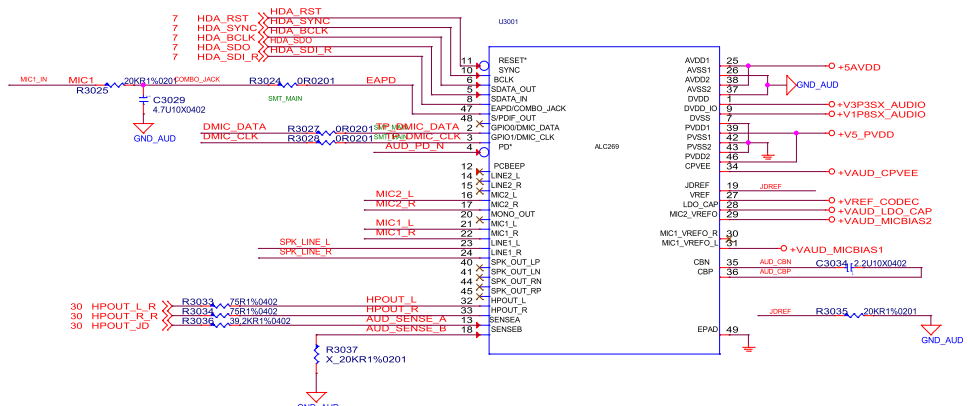
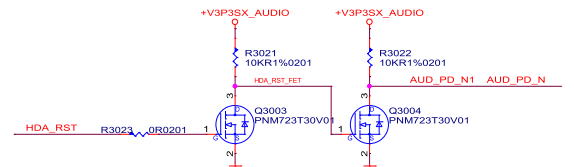
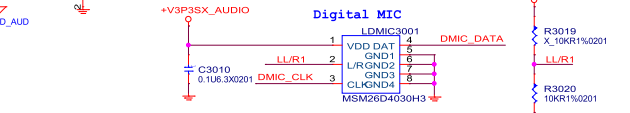
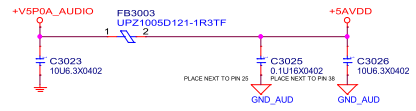
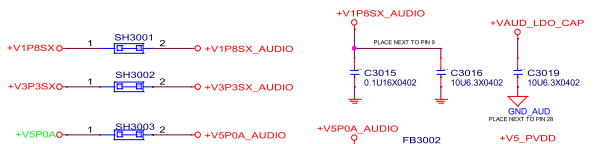
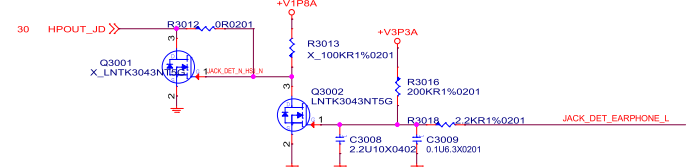
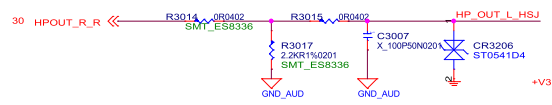
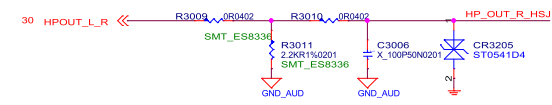
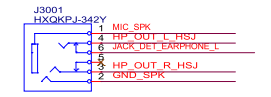
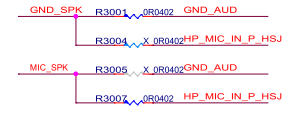
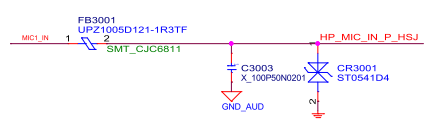
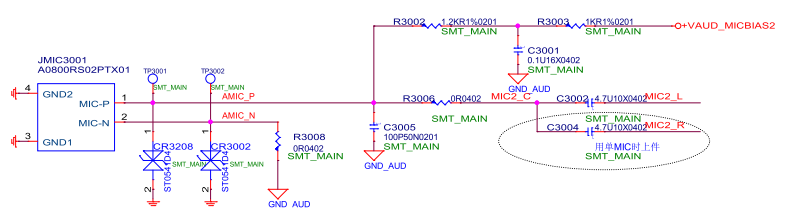




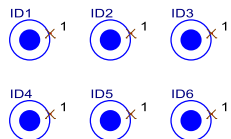
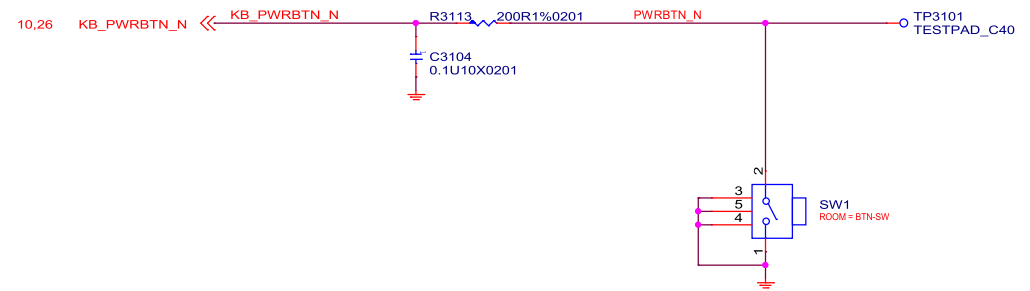
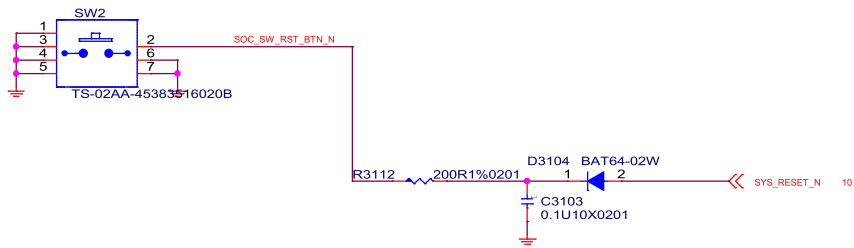
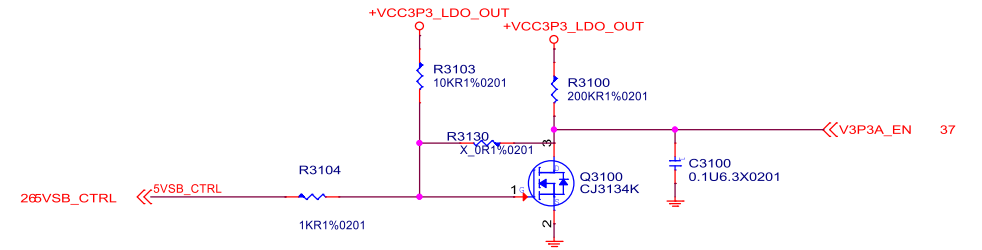
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PROJ	<b>youyeetoo X1</b>	
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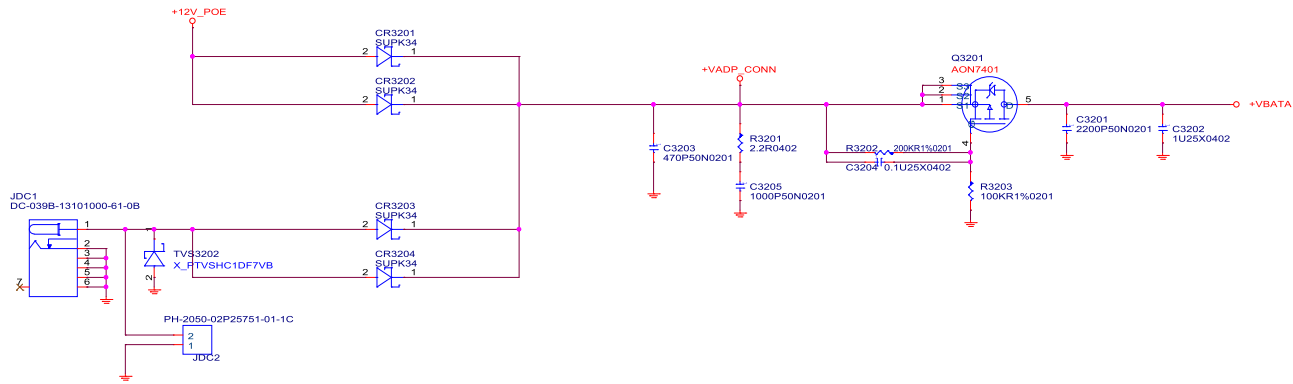


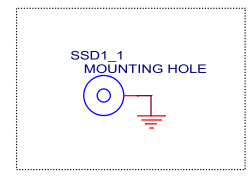
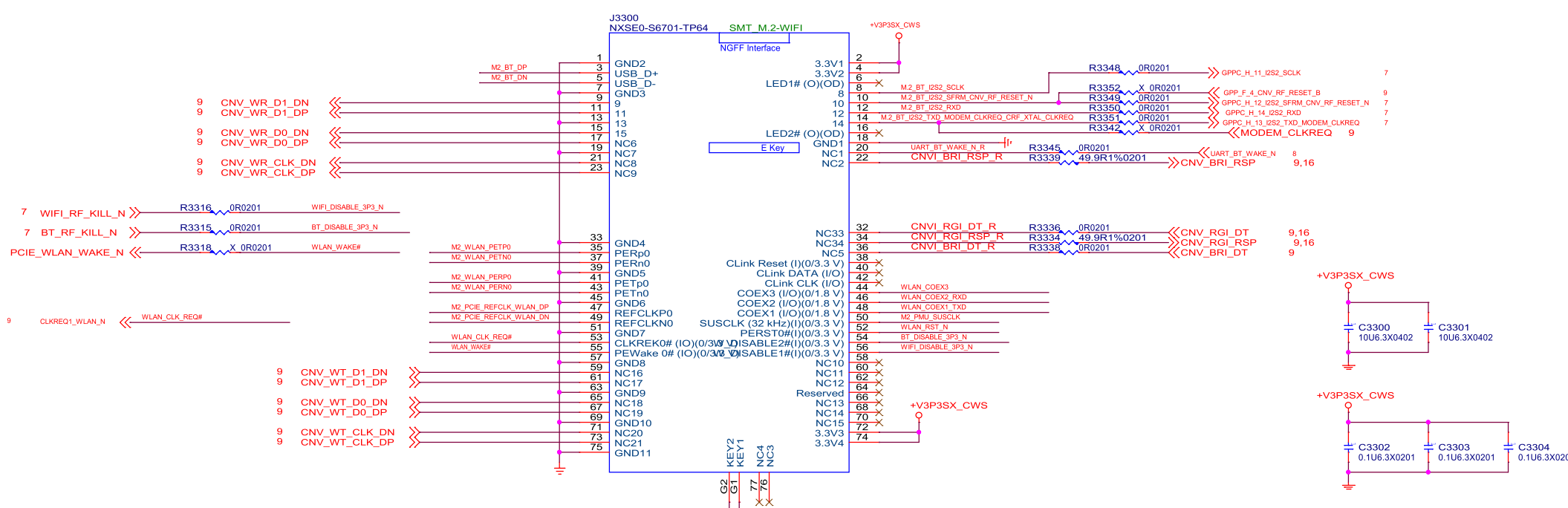
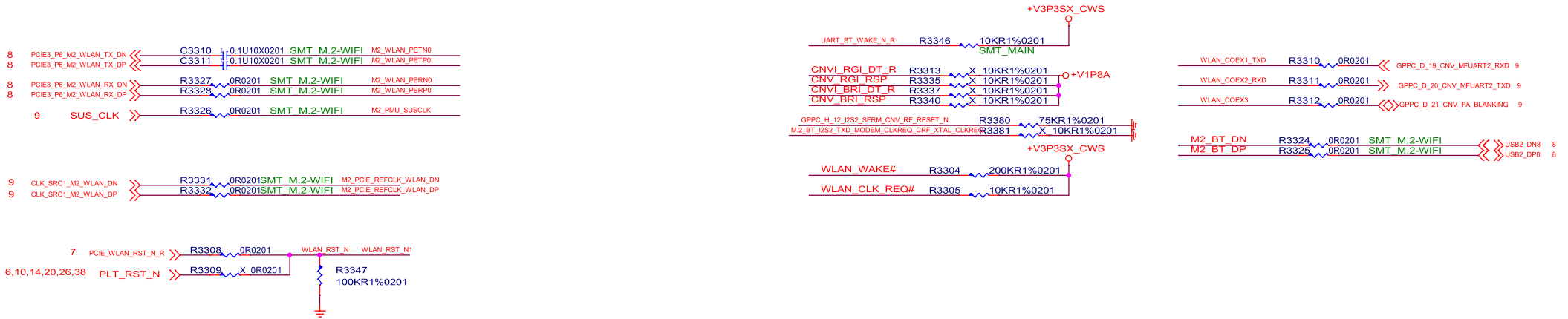


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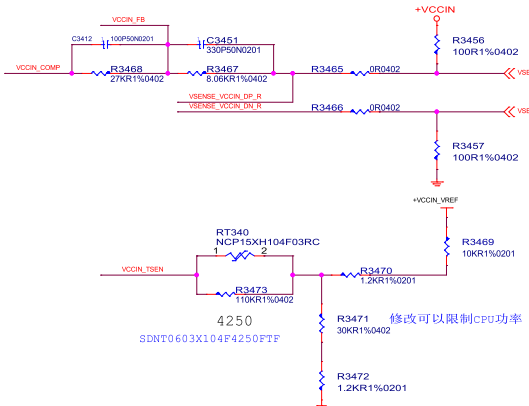
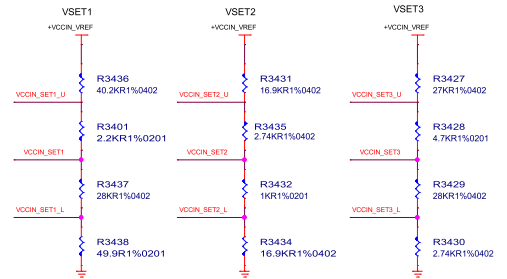
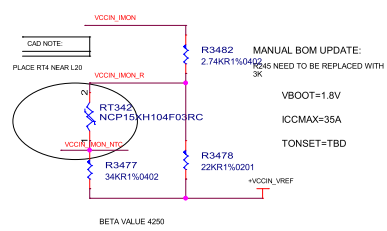
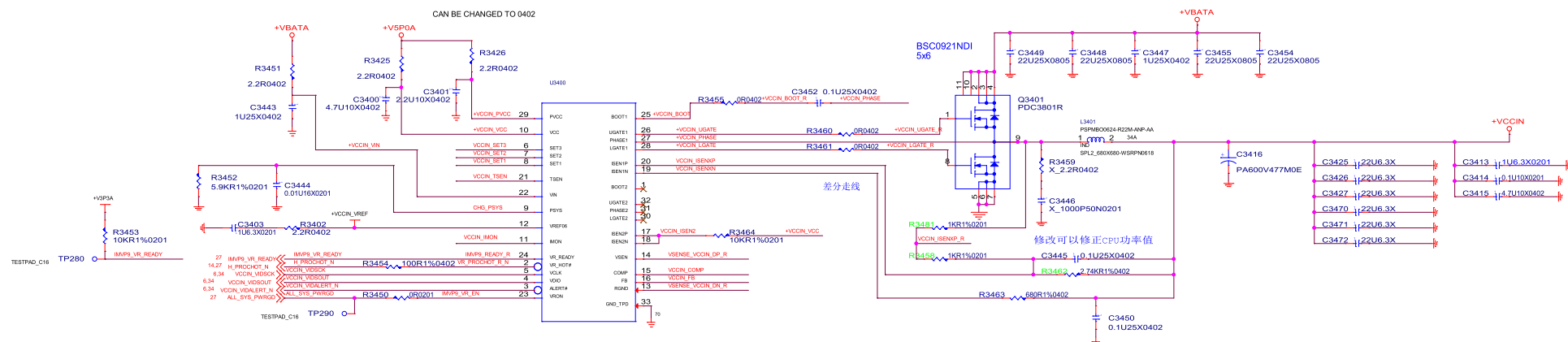
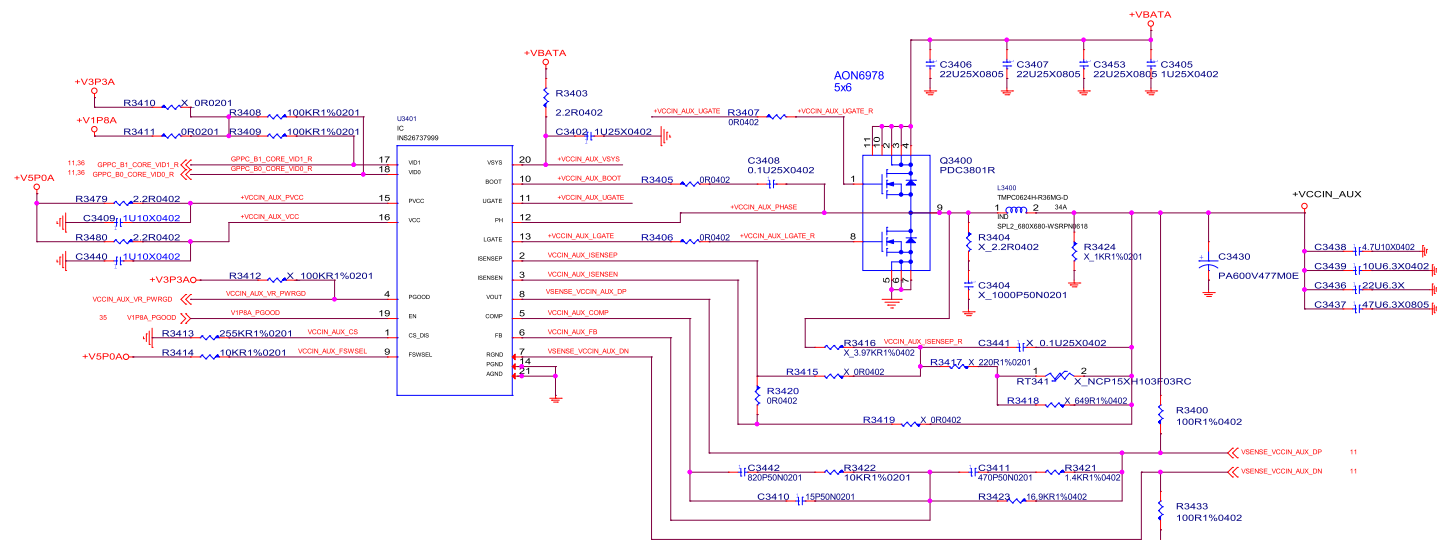


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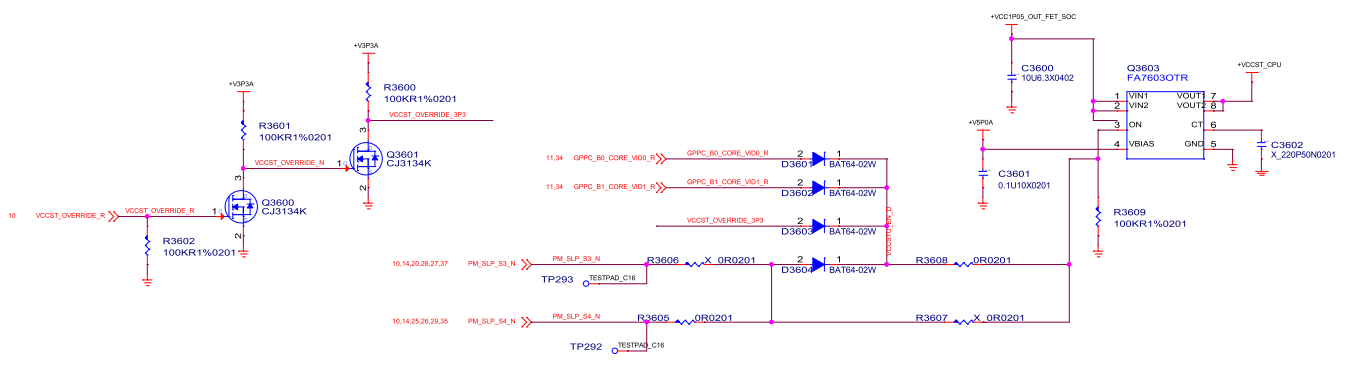


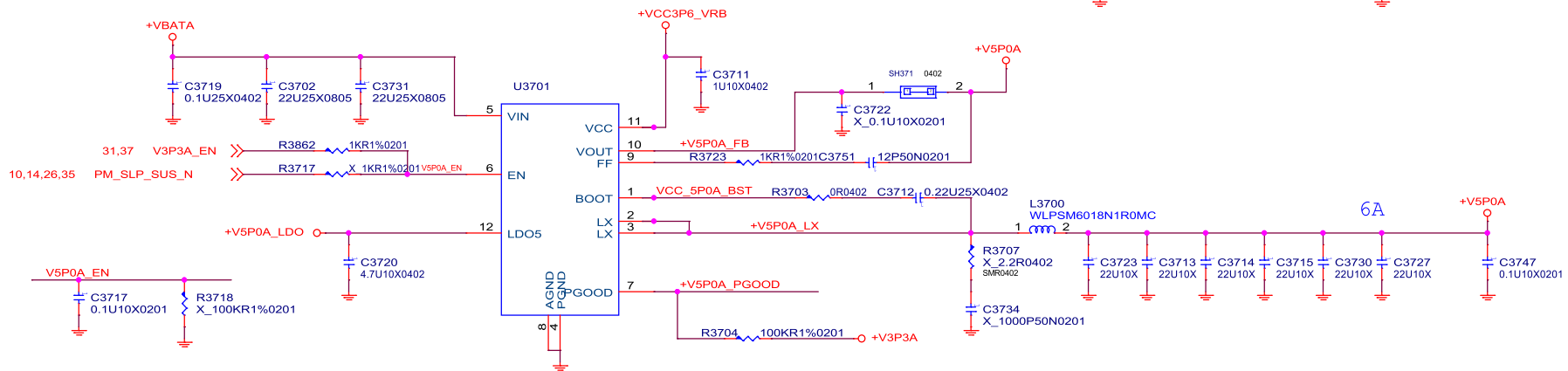
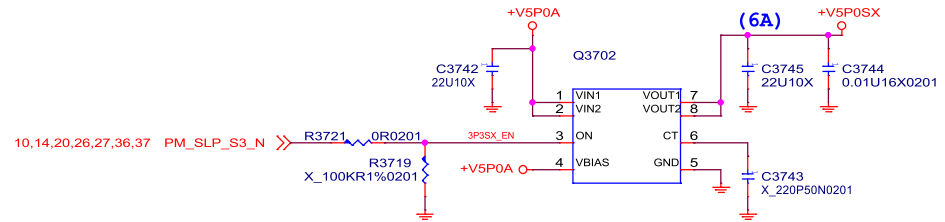
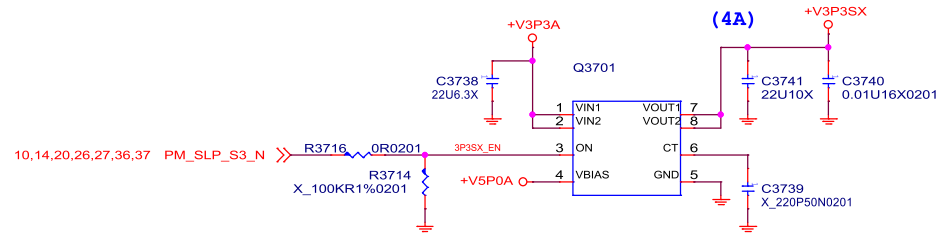
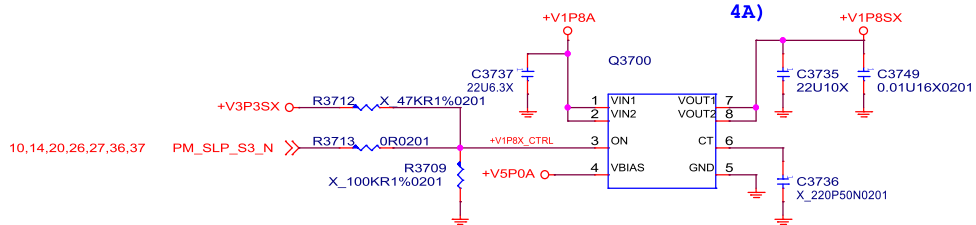
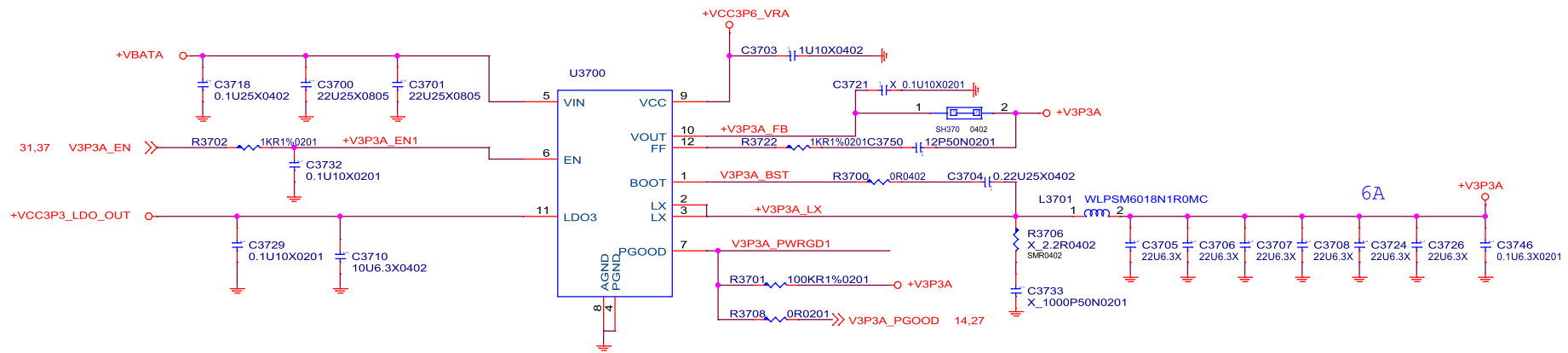


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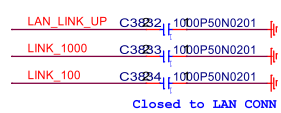
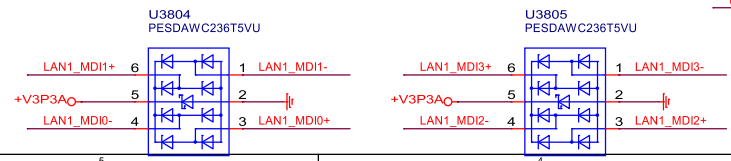
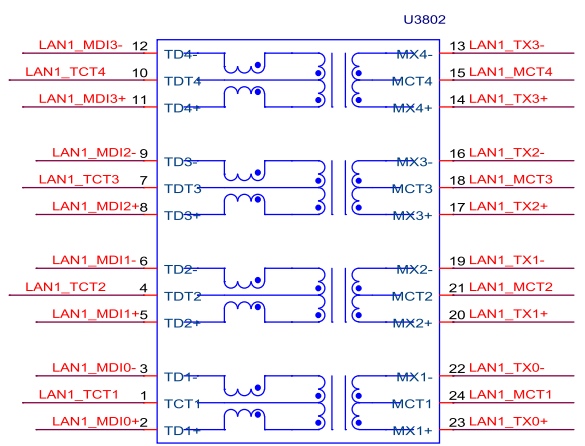
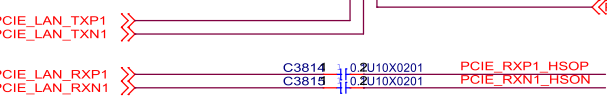
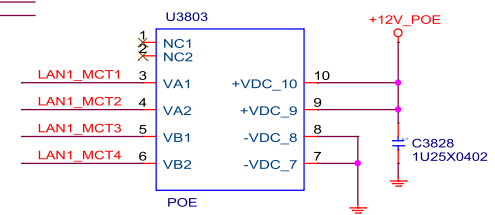
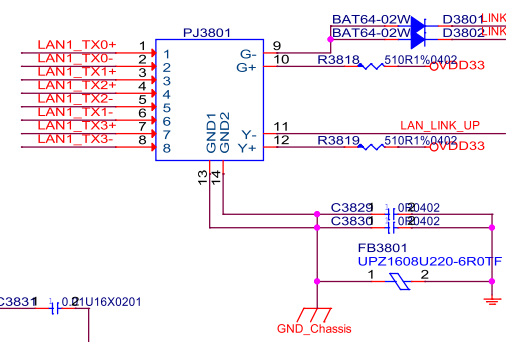
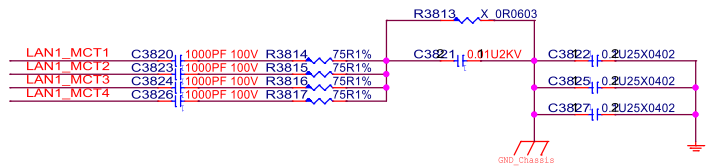
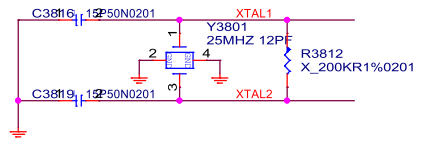
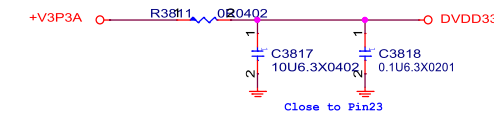
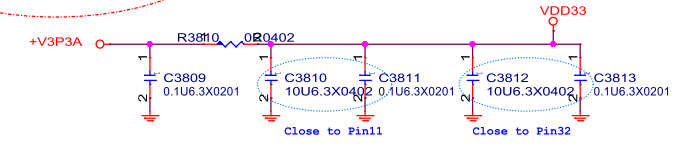
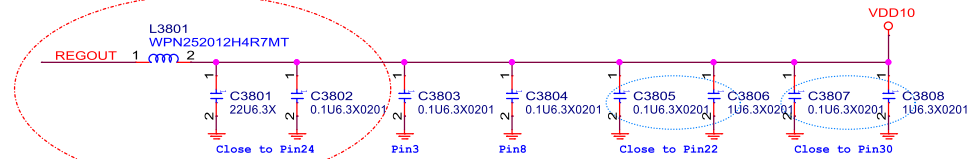
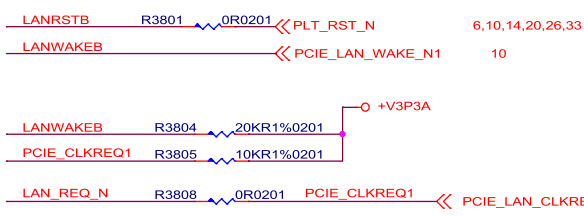
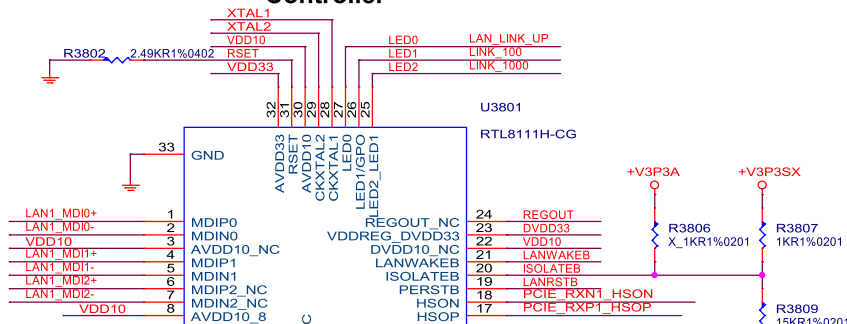






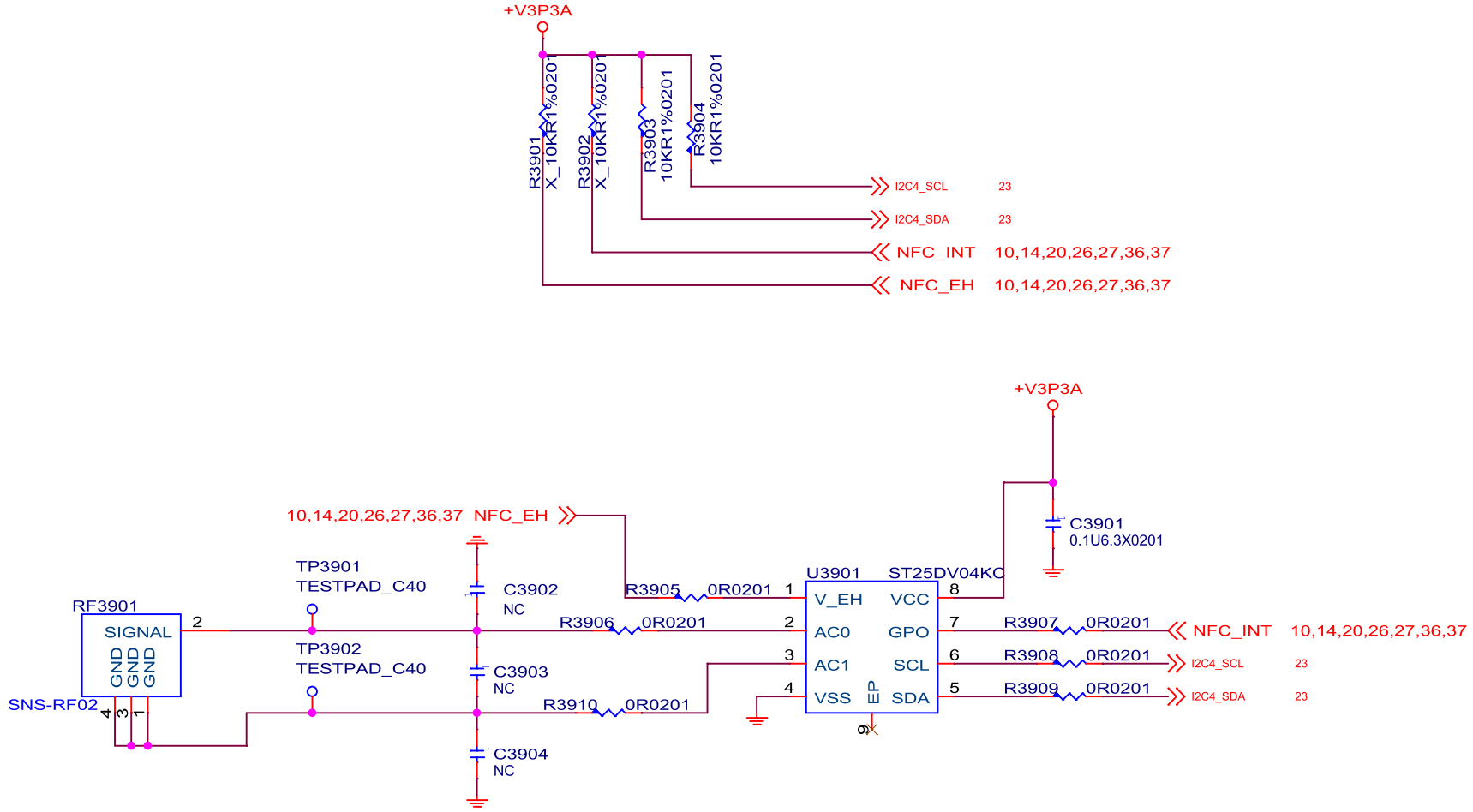
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